SYNOPSYS®

A Modern Solution for Analog/Mixed Signal Design

Recent Trends in AI-Assisted AMS IC Design - Workshop

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Agenda

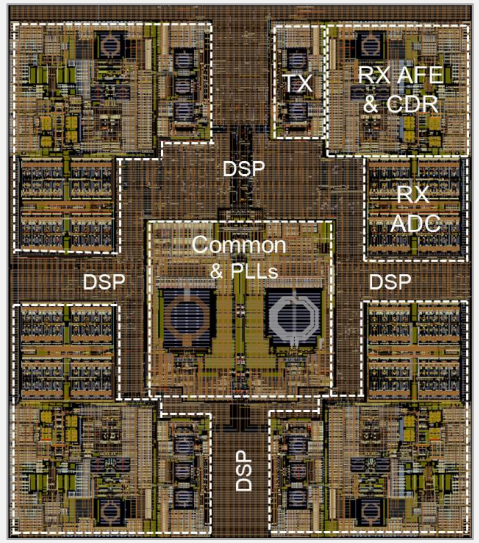
- Custom Compiler Overview
  - Schematic Editing
  - Layout Editing
- PrimeWave Design Environment
- PrimeSim Simulation
- ASO.ai: Design Optimization and Migration
- Cloud Solutions

Who I am

- Graduated in Microelectronics from University of Pavia with Prof. Franco Maloberti in 1996
- MBA from SDA Bocconi School of Management in 2007
- EDA “Grand Slam”, working in EDA since 1997
  - Mentor Graphics 1997-2000
  - Cadence Design Systems 2000-2021
  - Siemens EDA 2021-2023
  - Synopsys 2023-current

Customer Compiler Overview

Synopsys Offers a Modern and Proven Analog Design Platform



Analog

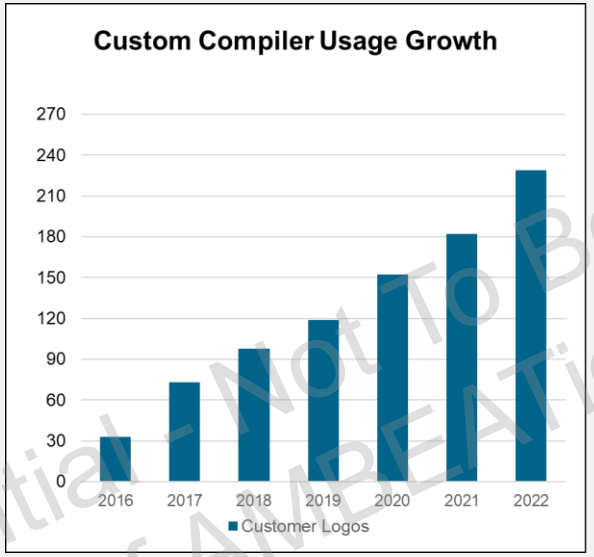
RF

Digital

Mixed-Signal

Used by #1 mixed-signal IP design team

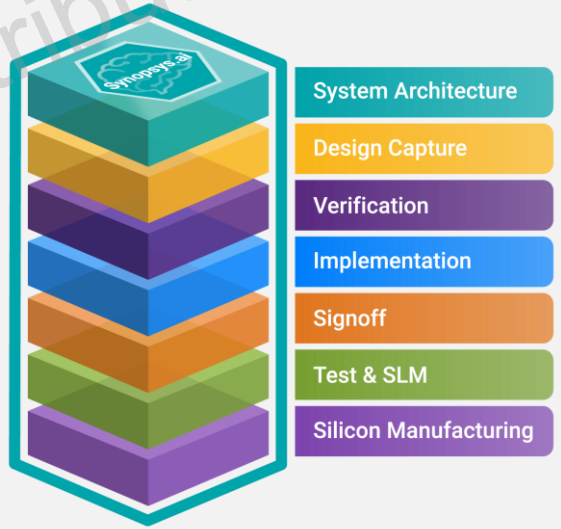
100's of new designs/year



Easy to adopt: Familiar use-model

200+ companies
3 of Top 5 HSIO IP

Synopsys.ai



AI-Driven Analog Design

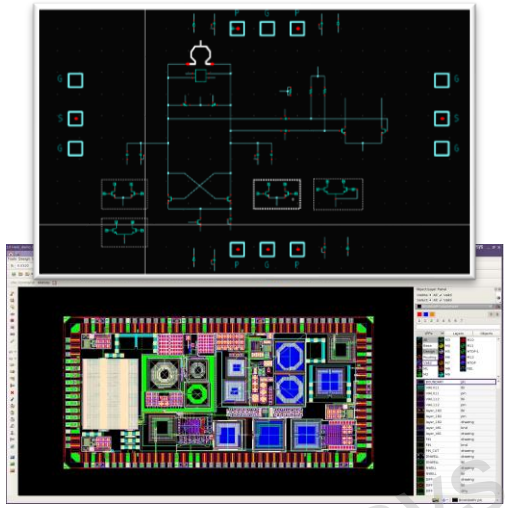
Faster closure
Design migration

Modern Analog, RF and Mixed-Signal Design Solution

Fully Featured AMS Design Platform

Design

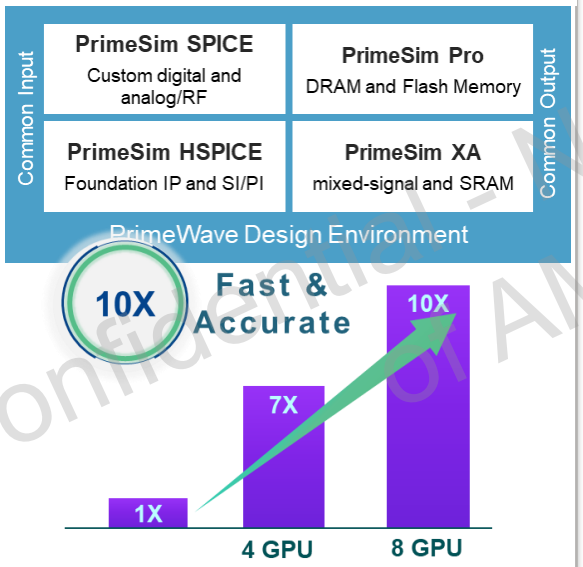
Custom Compiler



- **Schematic, Layout, P&R**
- **AMS Co-Design solution with Fusion Compiler**

Simulation

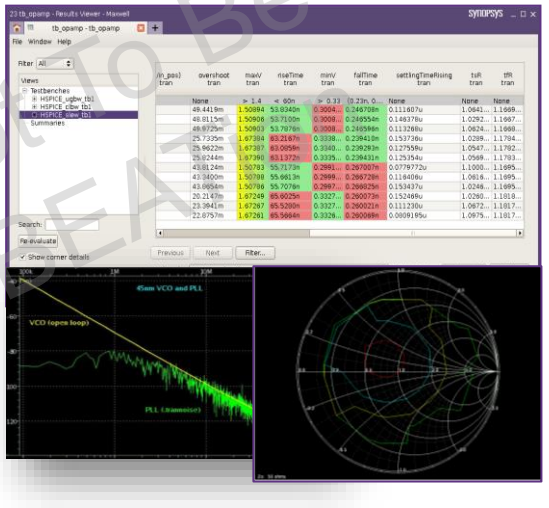
PrimeSim



- **Leading performance**
- **Golden accuracy**

Analysis

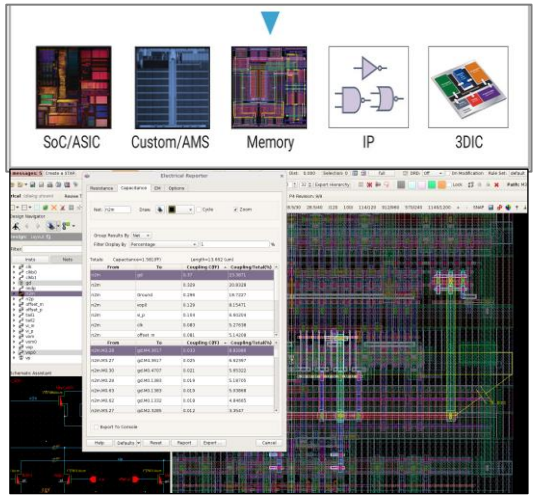
PrimeWave



- **Simulation, Optimization**
- **Reliability analysis and Design Robustness**

Signoff

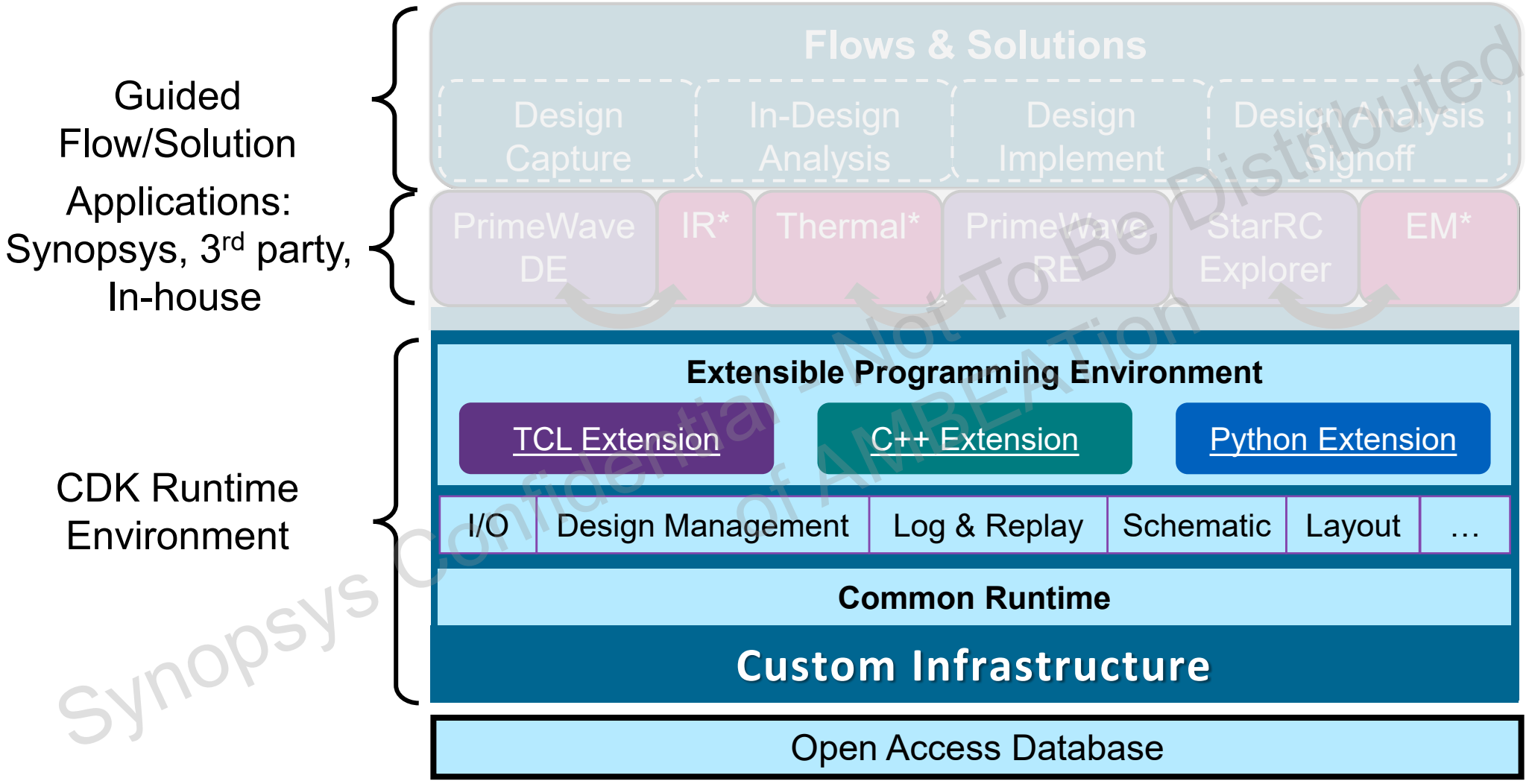
ICV & StarRC



- **In-design DRC/LVS/RCX**
- **Fusion technology for Integrated signoff**

Modern analog design platform, open for 3rd party integration

Open Custom Design Platform Ecosystem

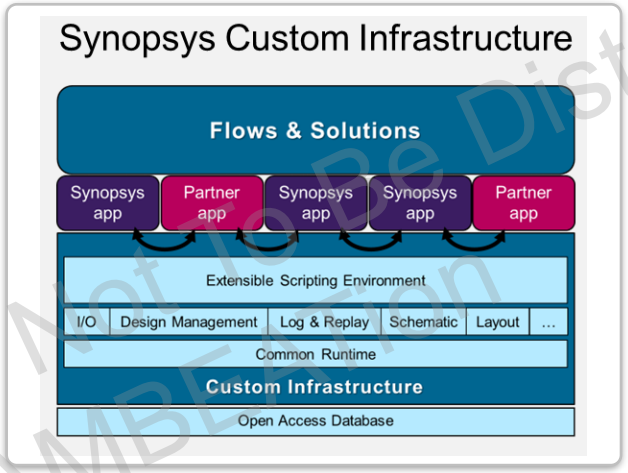


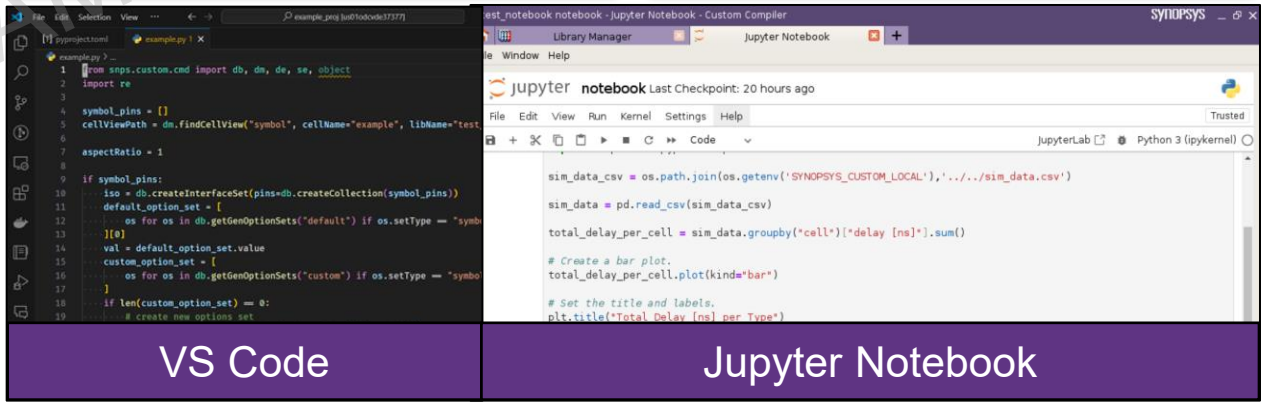
**Example Customer and Ecosystem tools for illustration*

Python Programming with Custom Infrastructure

Modern programming in an open design platform

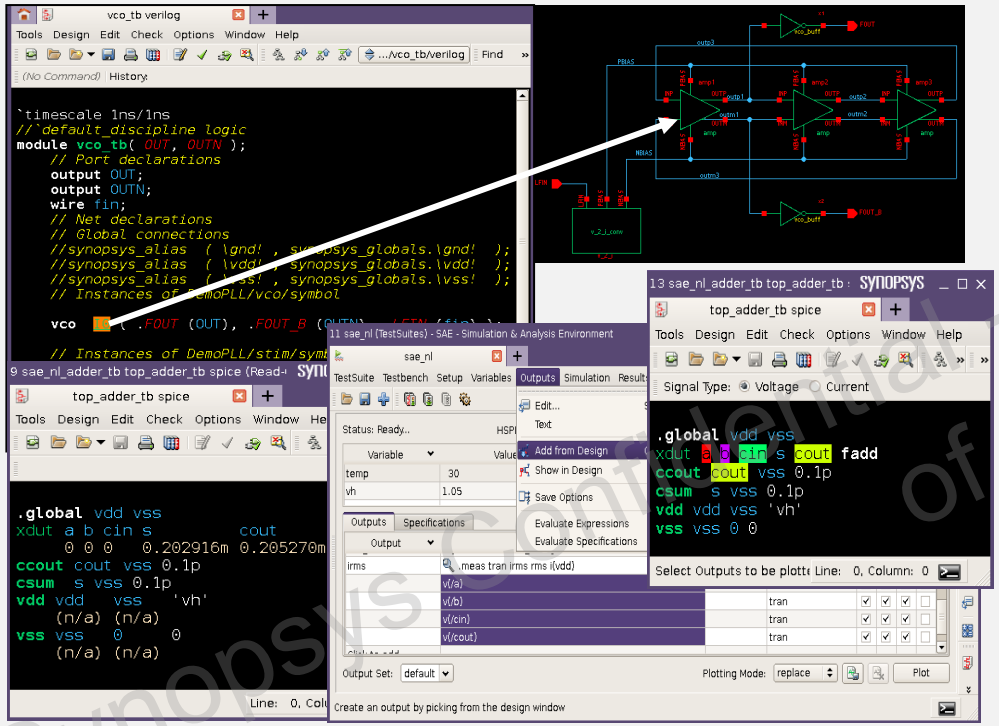
- Rich API library
- Native OA Python APIs
- 3rd-party Python libraries
  - Numpy
  - Pandas
  - Matplotlib etc.
- 3rd-party IDEs
  - Jupyter Notebook
  - VS Code





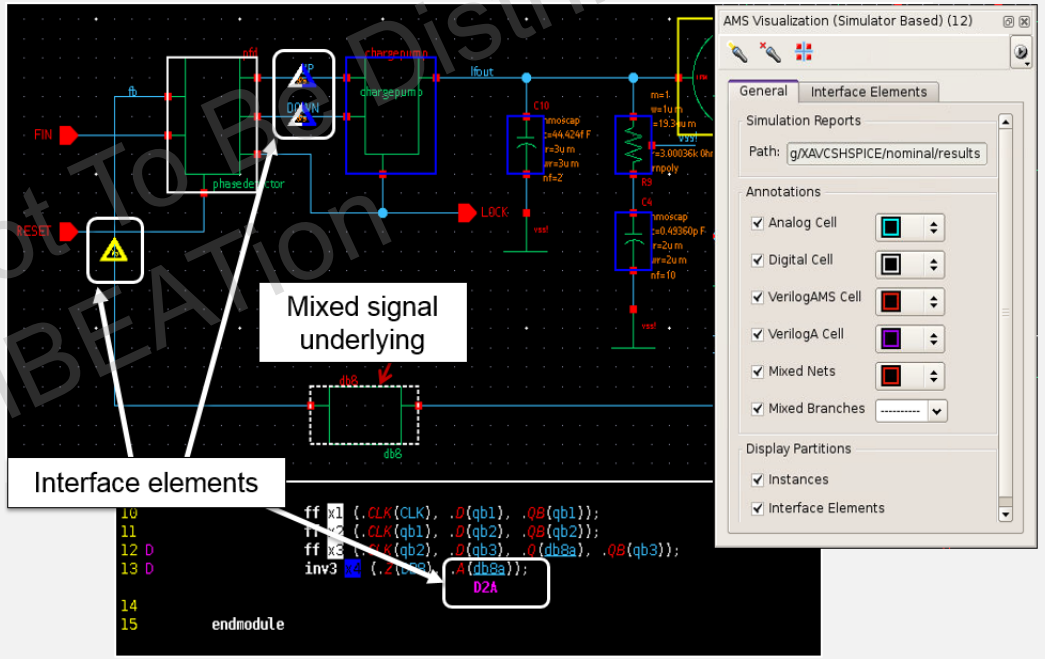
Schematic Productivity Features For Mixed Signal

Language Sensitive Text Editor



Cross-probing, back annotation, SRC/ERC to both text and schematic

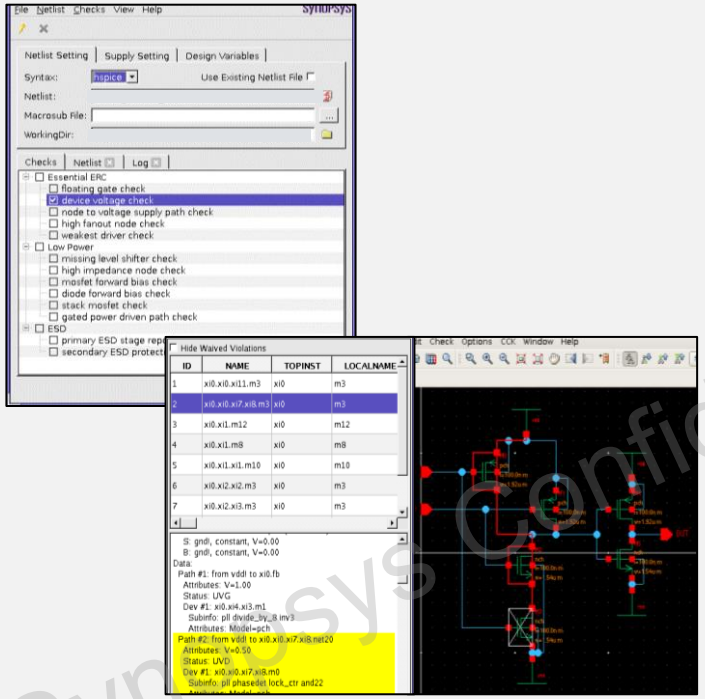
AMS Visualization and Debug



Automatic interface elements creation for A2D, D2A, E2R and R2E in both schematic and text

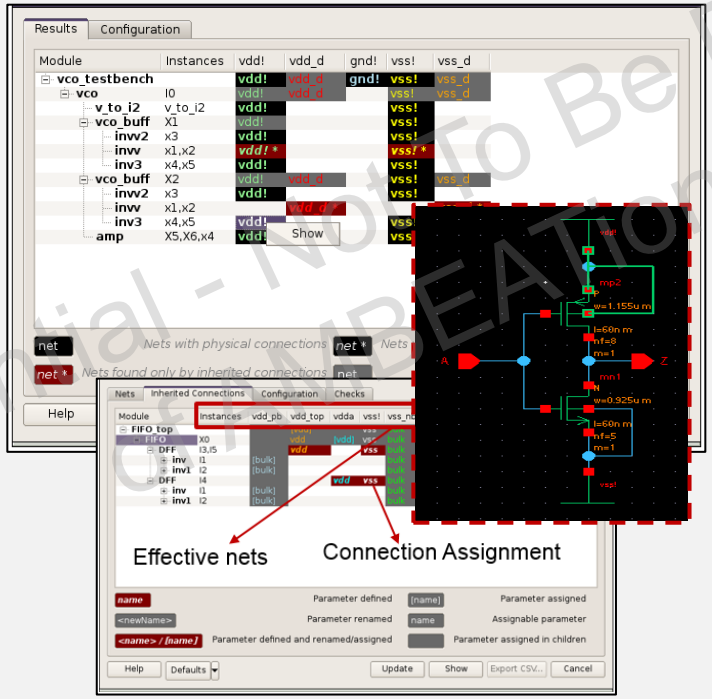
Schematic Debugging Capabilities

Transistor-level Circuit Analyzer



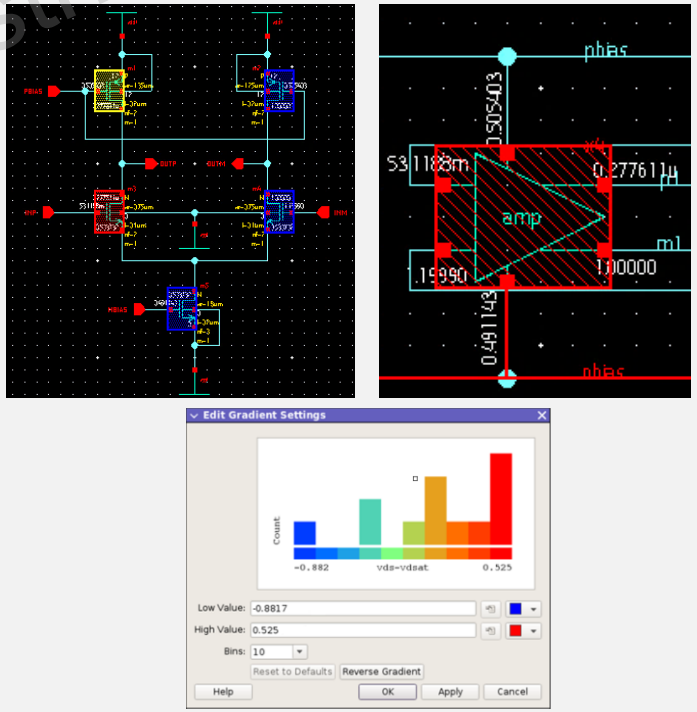
ERC, ESD & custom checks with schematic cross-probing, filtering and waiving

Power Domain Analyzer



Traces global nets through hierarchy
Analyze & debug inherited connections

Schematic Thermal Map

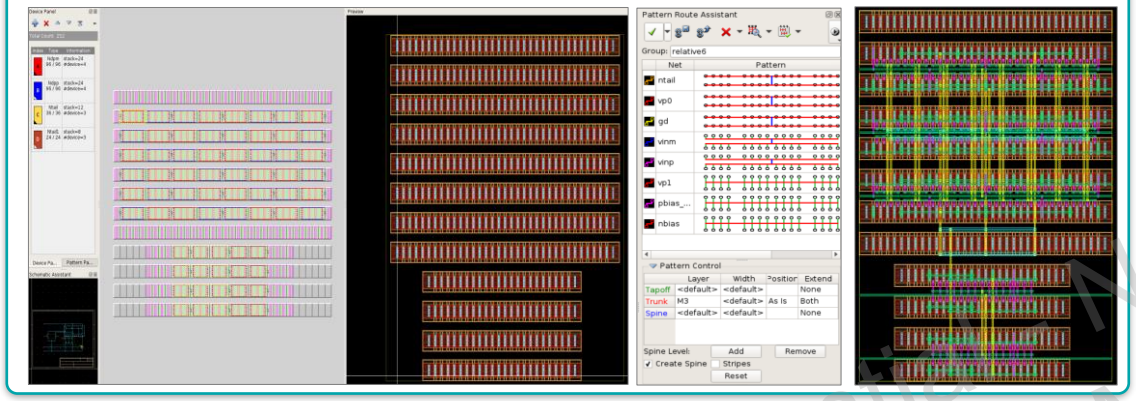


Thermal map annotations for operating points
Annotation propagation through hierarcy

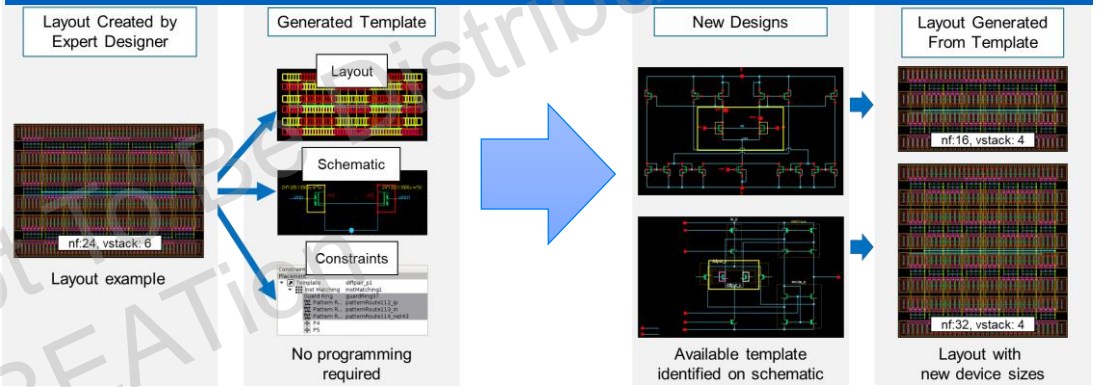
Custom Compiler Design Solution

Productivity: Features to speedup layout design

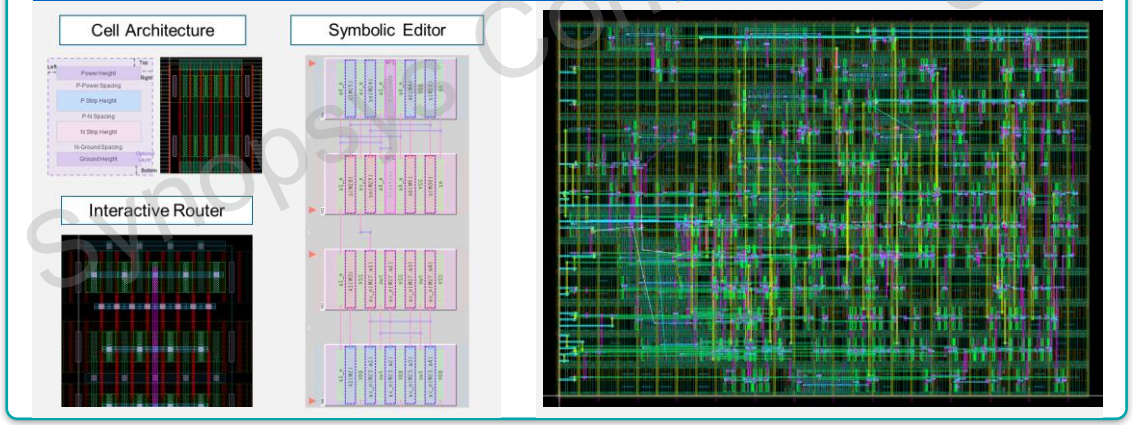
Visually Assisted Layout Automation



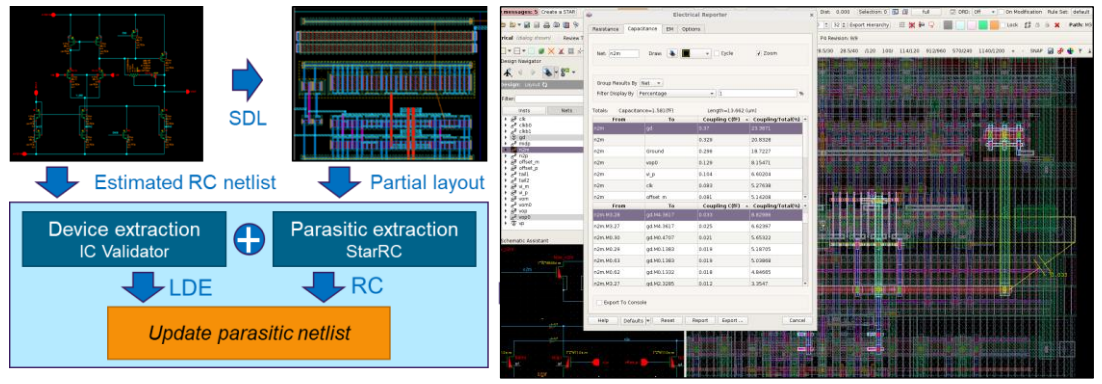
Analog Layout Reuse with Templates



Custom Digital P&R and Co-Design



In-Design Parasitic, EM/IR and DRC



Custom Compiler IC Validator Integration

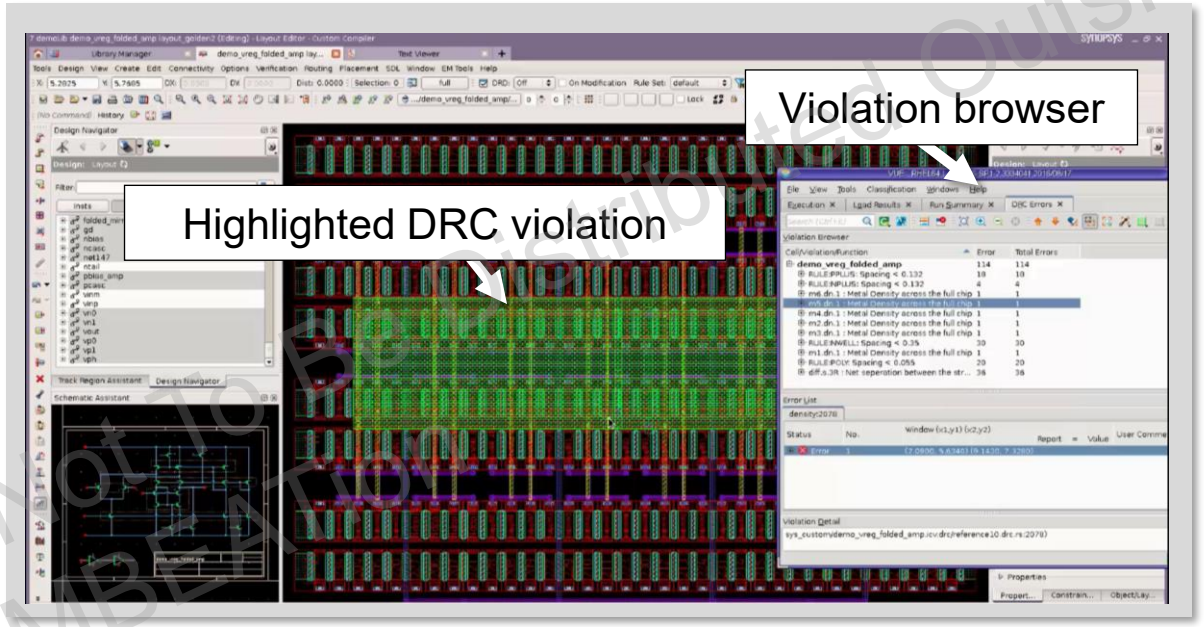
Signoff DRC and LVS

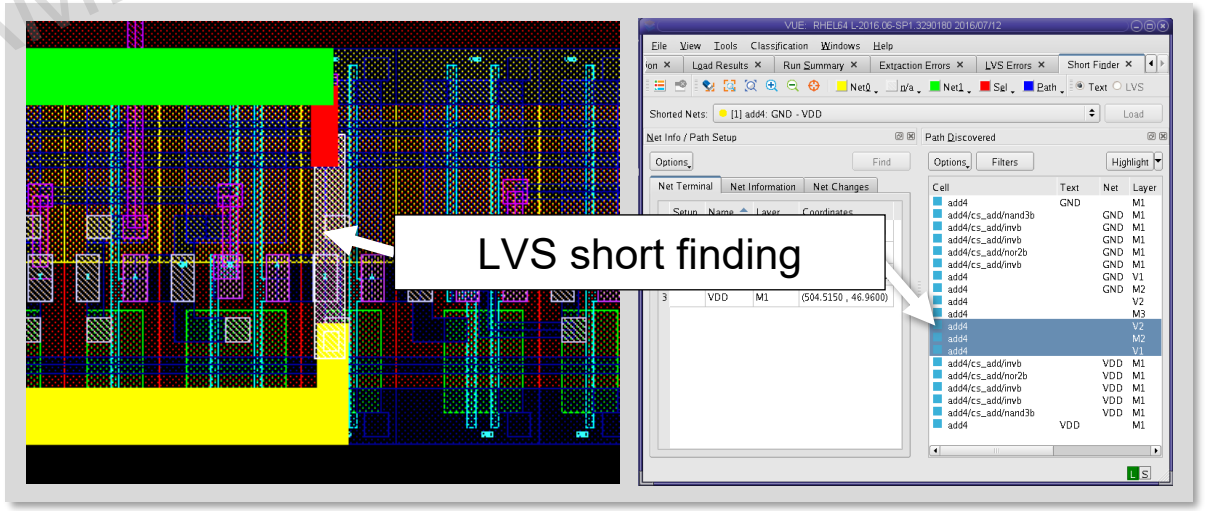
Fast, high capacity

- Multicore processing & multi-threading

Integrated with Custom Compiler

- Full cross-probing and debugging
- Runs directly on OA database
- VUE interface cross probe to schematic and layout
- OpenAccess native support





Custom Compiler StarRC Integration

Signoff Parasitic Extraction

Unified 3D fast field solver

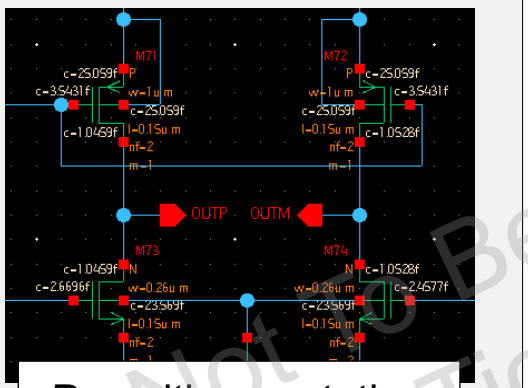
- Integrated 3D extraction
- Near-linear multicore scalability

Gold-standard accuracy

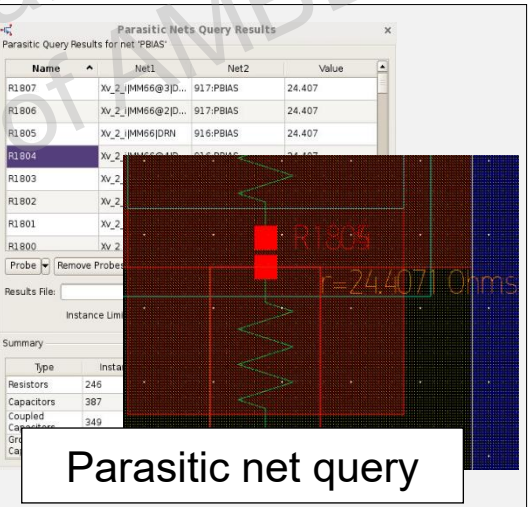
- Interconnect and layout-dependent device parasitic extraction
- Symmetric net extraction accuracy

Integrated with Custom Compiler

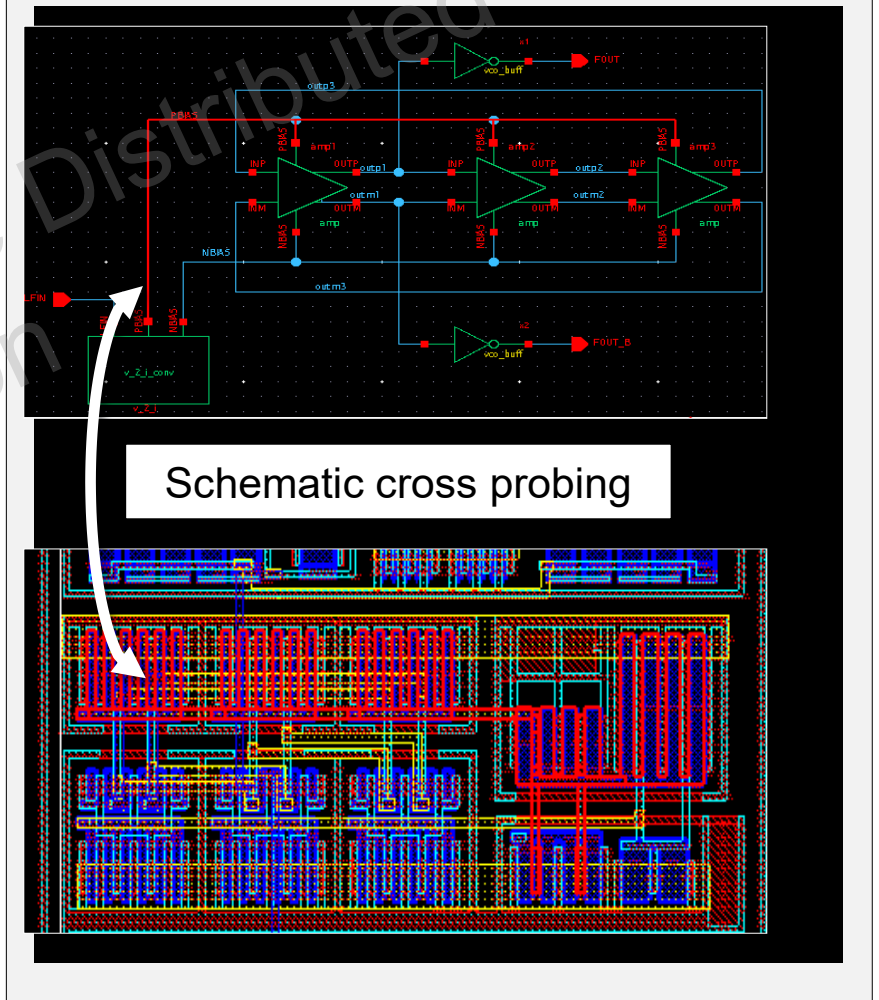
- Browse layout parasitics
- Netlist-out for post-layout simulation
- OA Extract view
- BackAnnotation of parasitic to layout and schematic views



Parasitic annotation



Parasitic net query



Schematic cross probing

PrimeWave Design Environment

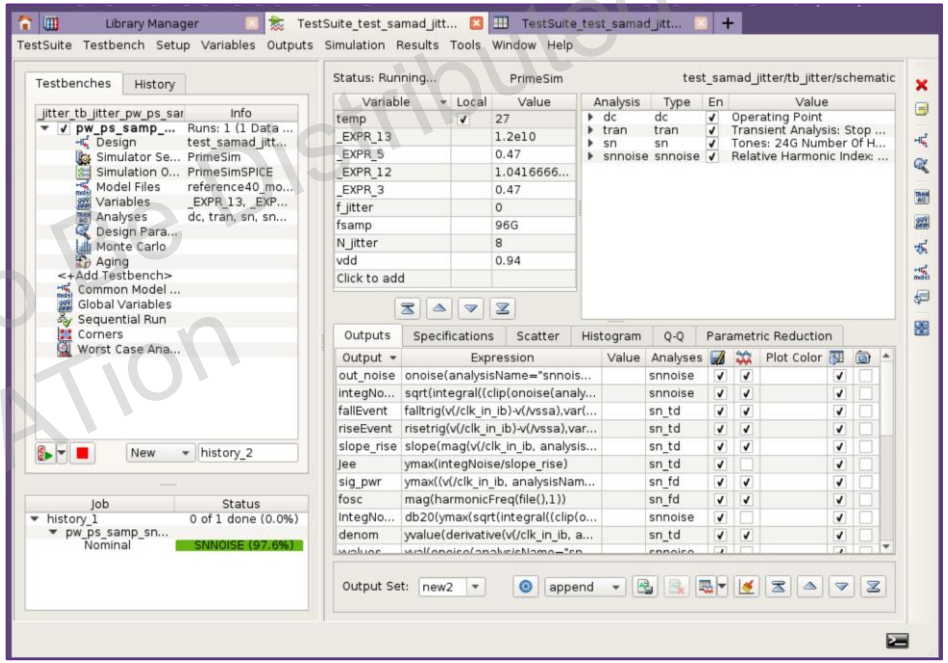
Simulation Environment and Waveform Analysis

PrimeWave Design Environment

A Modern and Open Simulation Environment

Comprehensive simulations and analyses flows

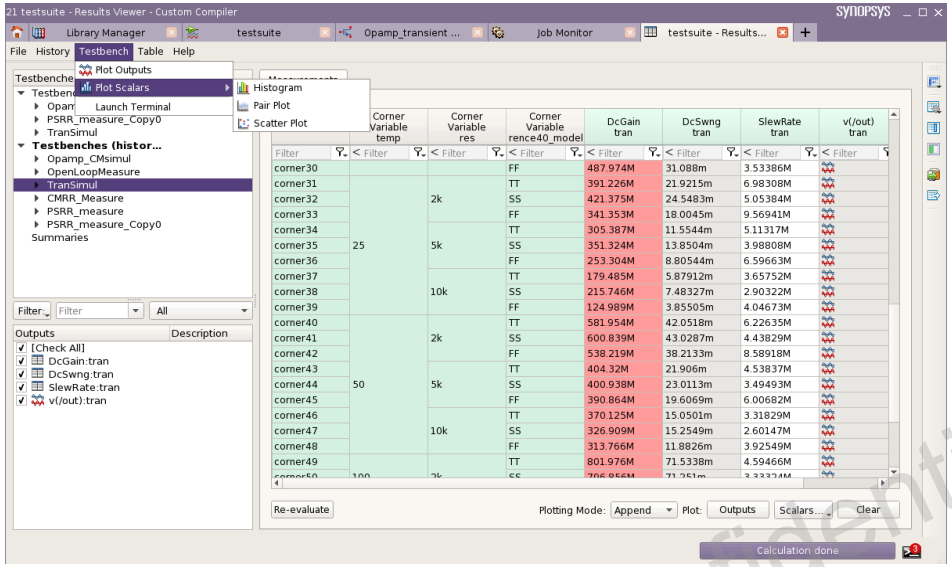
- **Corner analysis** with parameter sweeps
  - Focus on capacity and performance
- **Statistical analysis**
  - Monte Carlo with σ-amplification
- **Regression** Flow
- Design for Robustness
  - **EMIR, Reliability, aging** and **fault** analysis
- Complete **RF and noise** analyses
- **Mixed-signal** simulation
- **3DIC** and Multi Technology Model support



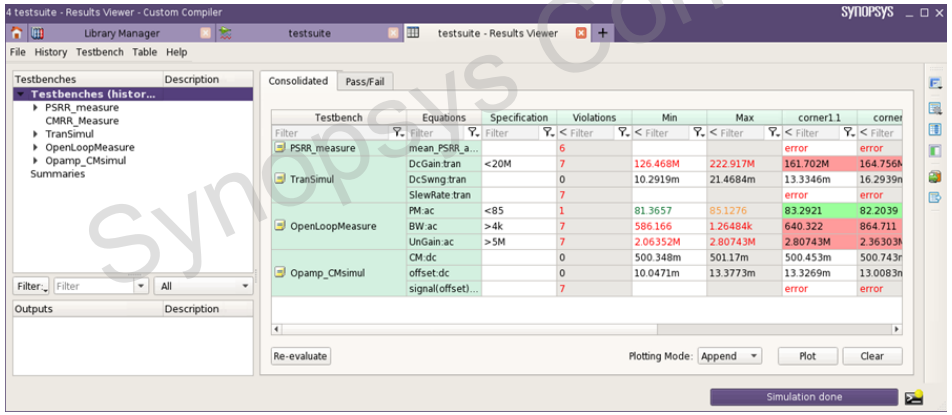
Designed for PrimeSim, works with 3rd Party simulators

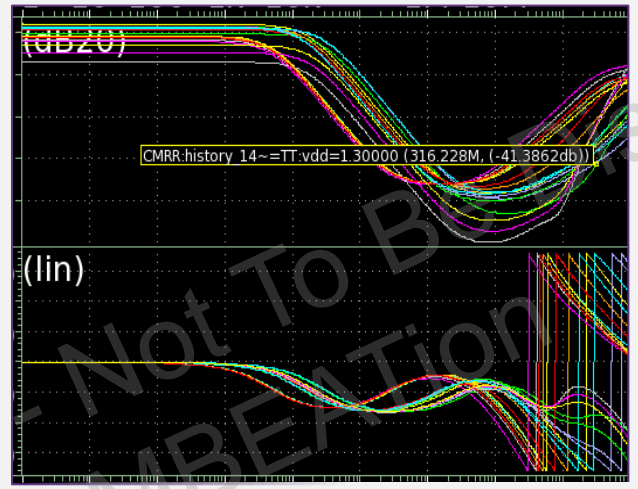
PrimeWave Design Environment

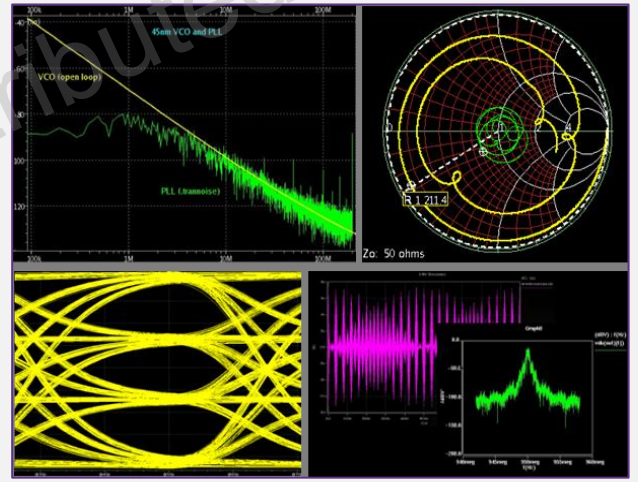
Analog, Mixed-Signal, RF Simulation and Analysis Environment



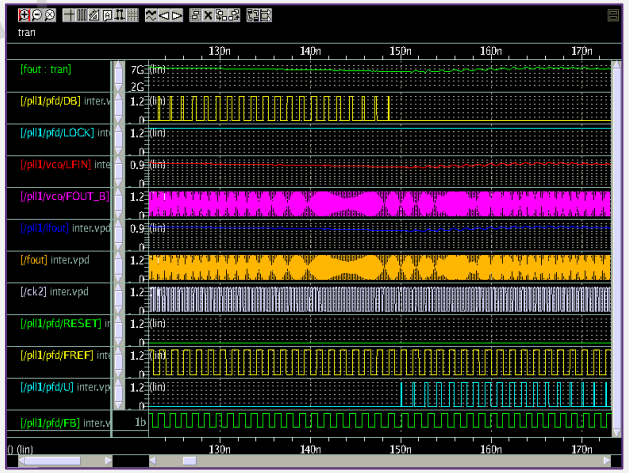
Multi-testbench results compare and display

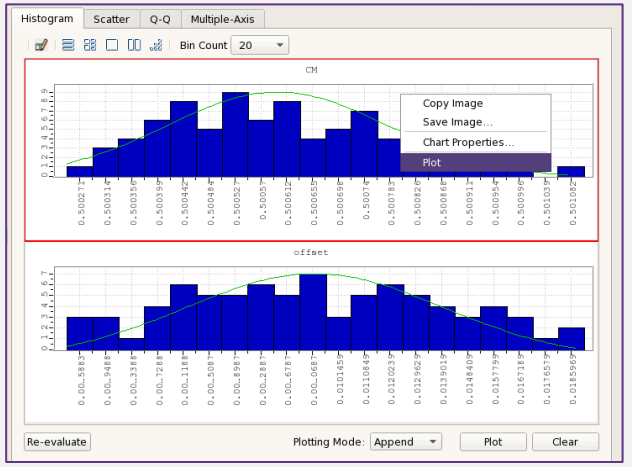






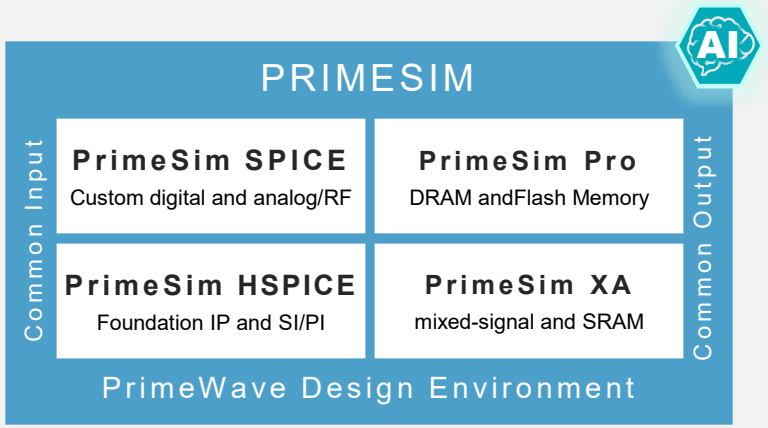
Fast, high-capacity waveform viewer





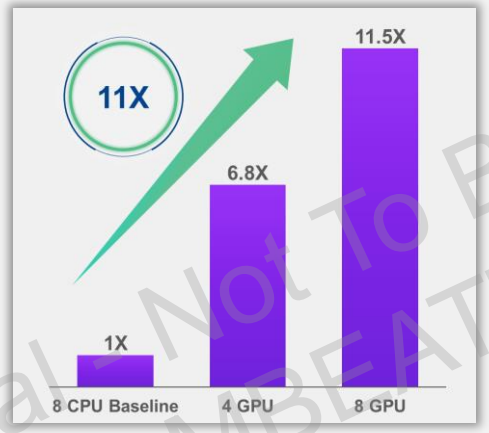
PrimeSim Update

PrimeSim: Next Generation Circuit Simulation Technology



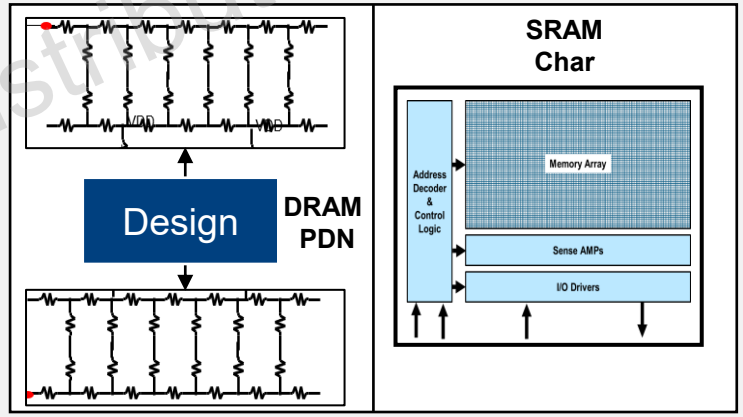
- Unified workflow of best-in-class simulation engines
- Modern and open design environment

SPICE



- Proven for Analog & RF, **2-5X** faster vs. competition
- **10X** speedup with GPU (A100/H100) for post-layout

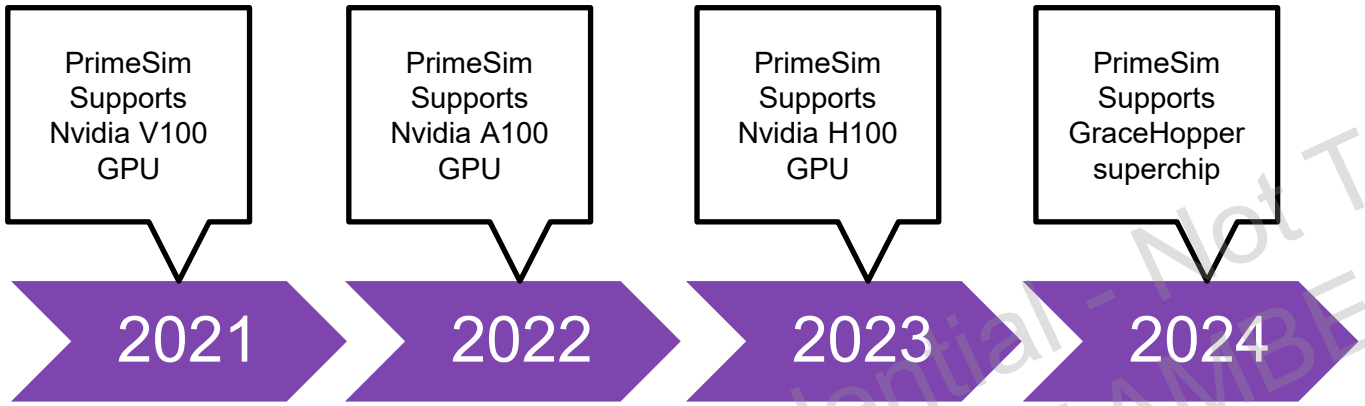
FastSPICE

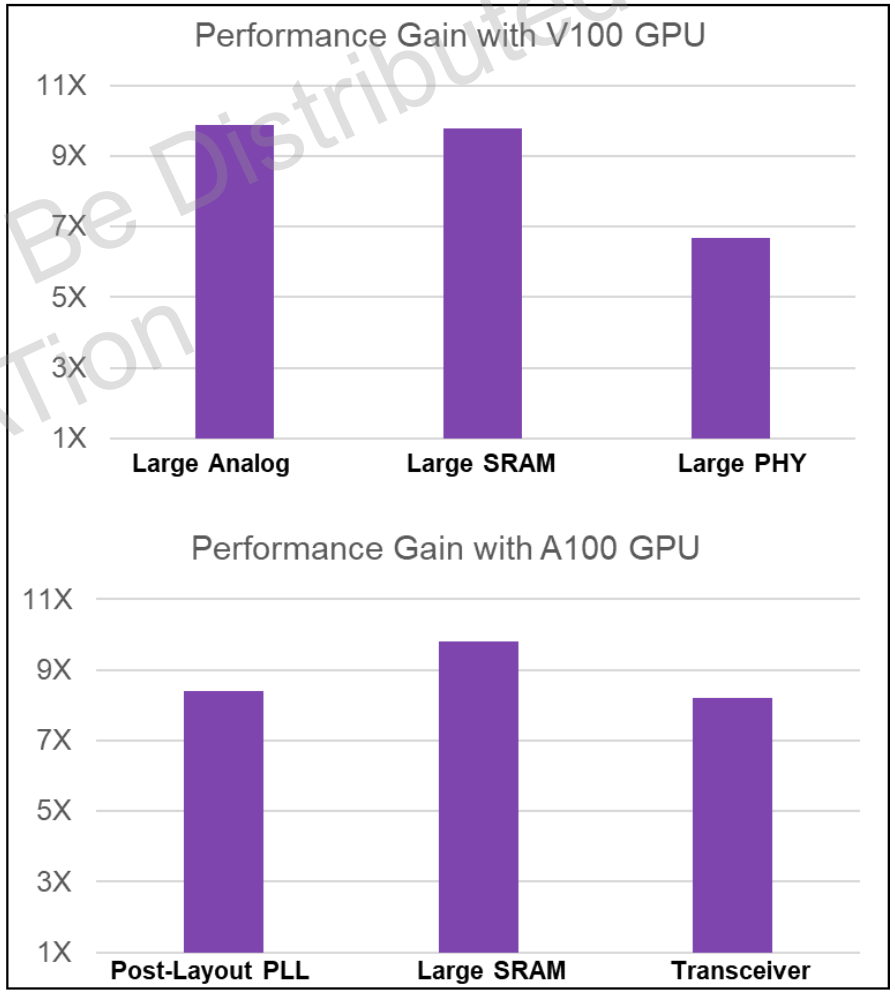


- DRAM PDN: **8X** speedup on CPU; addl. **5X** on GPUs
- SRAM Char.: **3X** speedup for N3/N4

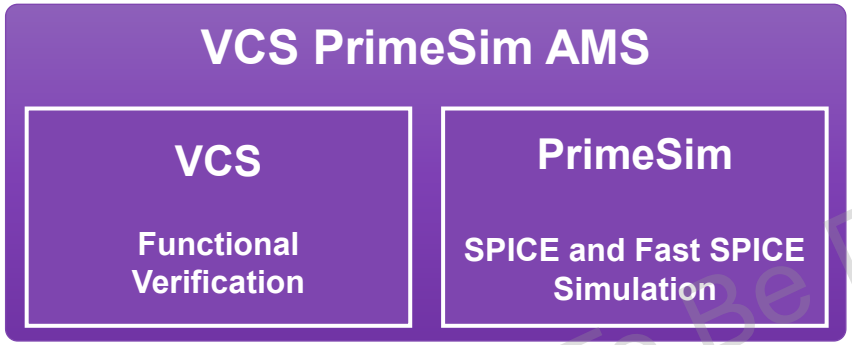
AI-driven design retargeting and high-sigma variation analysis

Industry’s Only Proven GPU Accelerated SPICE Simulator





Robust Mixed-signal Verification for Higher Coverage



Fast

- Direct Kernal Integration (DKI)
- Multi-core scalability
- RTVS (Real-Time View Swapping)
- GPU acceleration

Flexible

- Comprehensive model support, Verilog-A, Verilog-AMS, SV, RNM
- Support for user-defined and pre-defined SV Nettypes, including VIZ

Low Power

- Unified UPF methodology for mixed-signal designs
- Easy configuration of power for Interface Elements/Connect Modules

Easy Debug

- Single FSDB file for AMS debug and waveform viewing
- Flexible save and restore capabilities
- Informative diagnostic reports

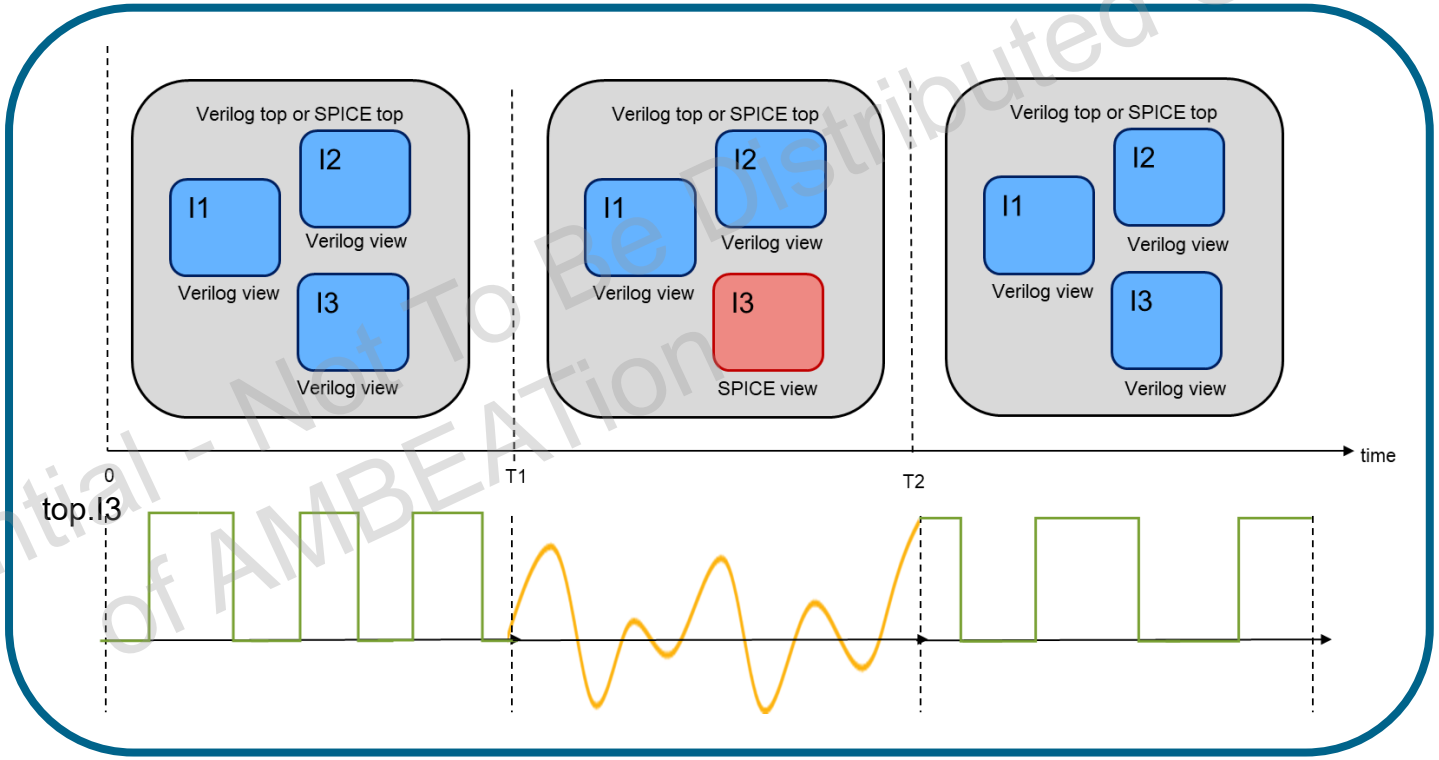
Advanced SoC

- Full-chip SoC verification
- Seamless connectivity between A/D
- Advanced analyses support: fault, rail, variation, and aging

Performance Acceleration Beyond Traditional Co-Simulation

2-6X Faster

- Real Time View Swapping (**RTVS**)
- Allow dynamic swapping between analog and digital views during simulation
- Provide flexibility to choose accuracy and performance



Testcase	Standard Co-Sim	RTVS	Speedup
Case 1	8.19 hr	1.34 hr	**6.1x**
Case 2	5 hr	1 hr	**5x**

Introduction to ASO.ai

Design Migration and Optimization

What's ASO.ai?

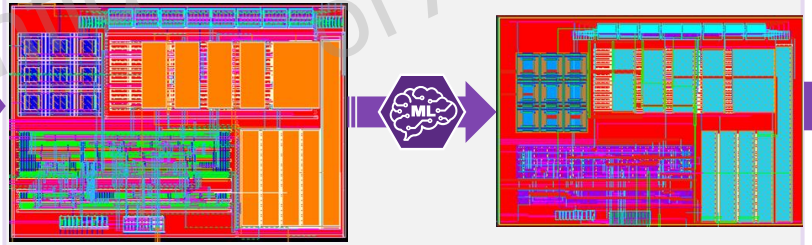
AI-Driven Analog Design Solutions

Supported by Leading Foundries

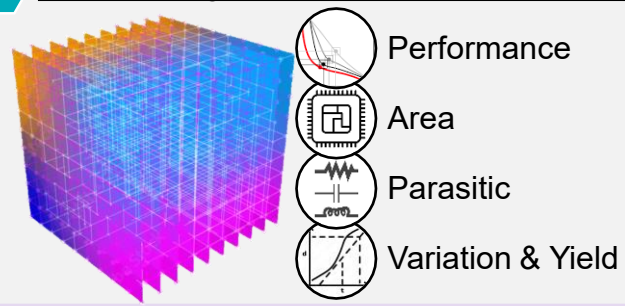
intel SAMSUNG tsmc

Schematic Porting

Rapid Layout Migration



Multi-Objective Optimization



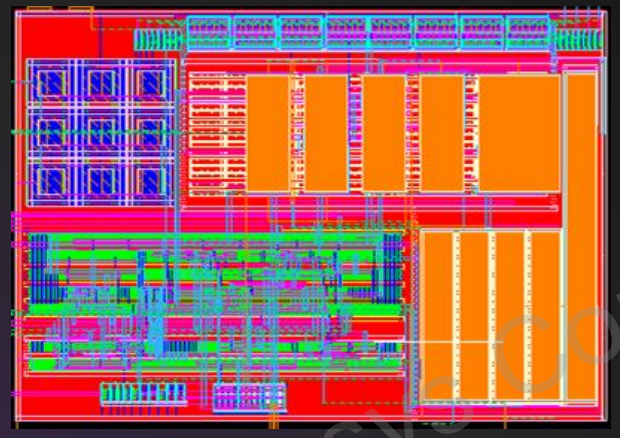
2X – 4X Faster
Analog IP Node Migration

5X – 10X Faster
Analog Circuit Optimization

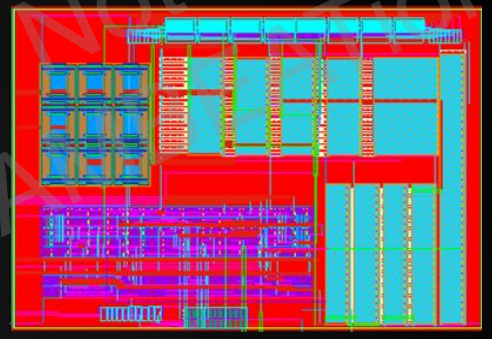
Accelerating Analog IP Migration with ASO.ai

ASO.ai Faster Time to Results: Analog IP Migration and Design Optimization

Current Node



Target Node



22nm Analog IP	2-3X Faster Layout Migration
22nm mmWave PA	10X Faster RF Design Migration
7nm Connectivity IP	8X Faster Time to Optimized Circuit
Special Node Memory	2-5X Faster TTR Layout IP Node Migration
GAA Analog IP Team	2-4X Faster TTR IP Node Migration

tsmc intel SAMSUNG GlobalFoundries TOSHIBA KIOXIA RENESAS CREDO we connect.

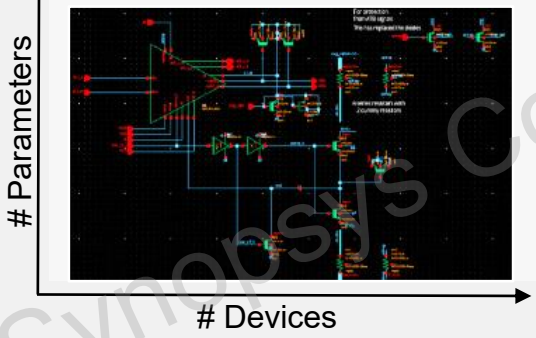
ASO.ai: AI-Driven Circuit Optimization

Multi-Objective **A**nalog Design **S**pace **O**ptimization Solution

Center Schematic → **Optimize** With Parasitics → **Optimize** High-Sigma

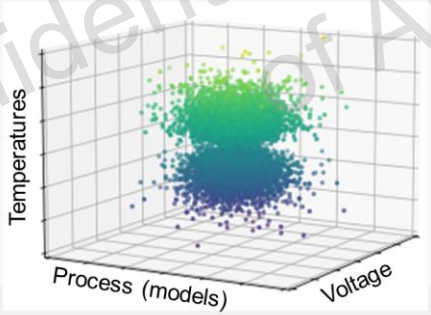
Dynamically learns through simulations experiments

Devices & Parameters



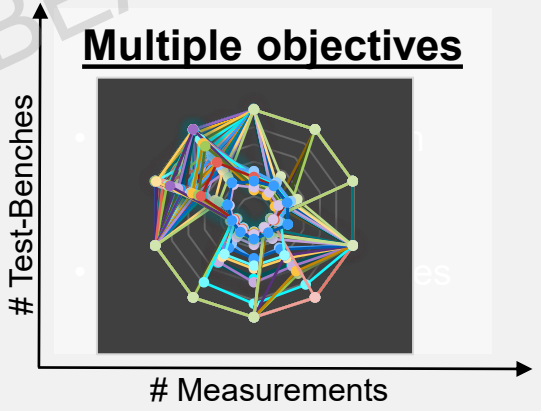
X

1000's PVT Corners



X

Multiple objectives



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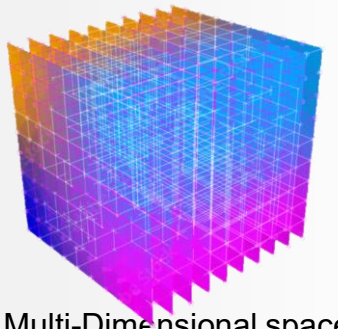
Large Design Space



Multi-Dimensional space

Intelligently explore of an extremely large design space to quickly optimize analog circuits

Custom Compiler Design Platform

ASO.ai: Analog Design Migration Solution

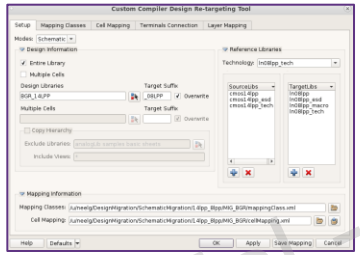
Front-End Design Porting

Layout Migration

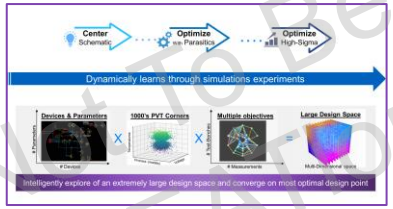
Setup

- Devices and Parameters mapping
- Technology mapping
- Verify LVS
- SDL View (layout connectivity)

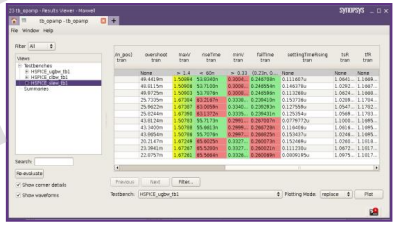
Schematic Porting



Optimization

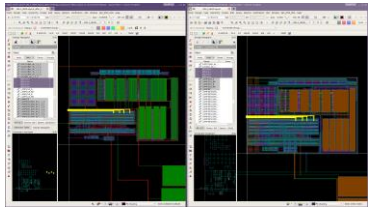


Verifications



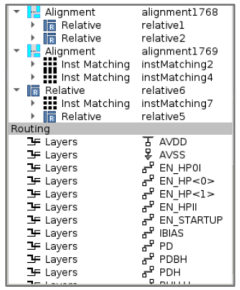
Review

- Reports / Docs
- Layout compare

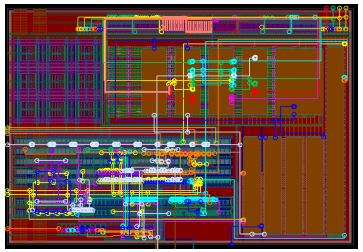


- Physical verification
- OA, GDS, DSPF

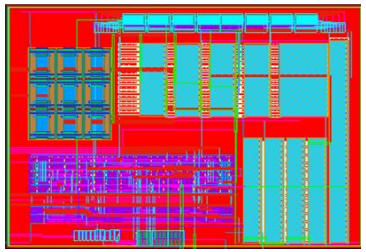
Source learning



Layout Migration



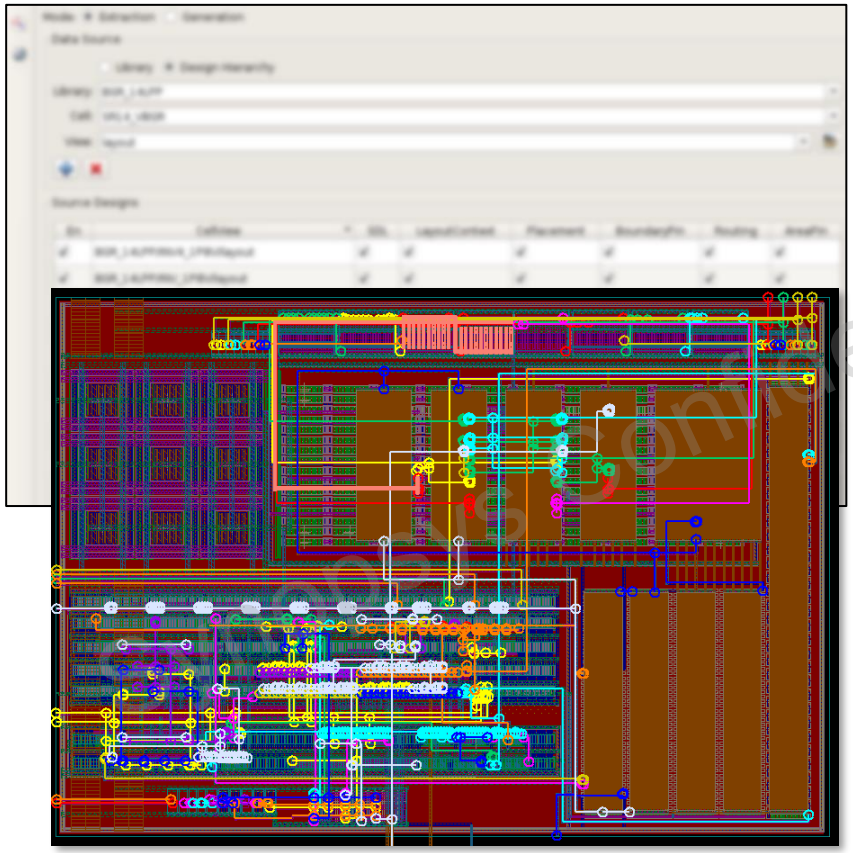
Layout Finishing

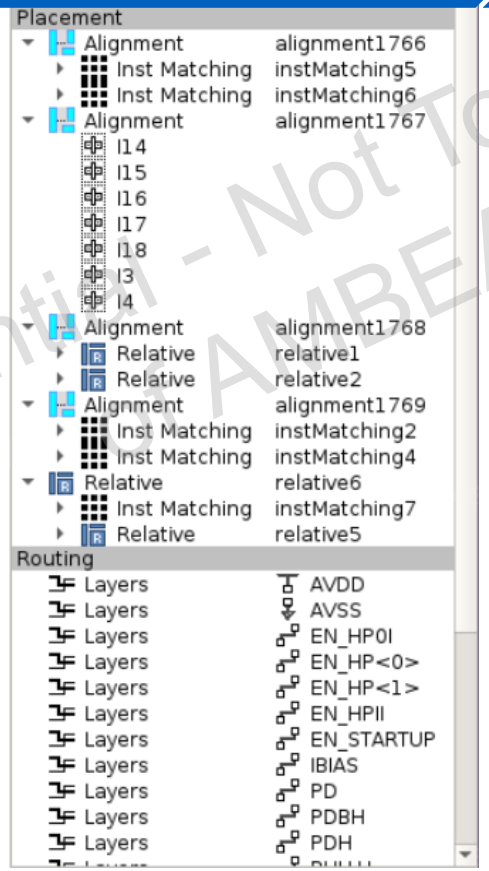


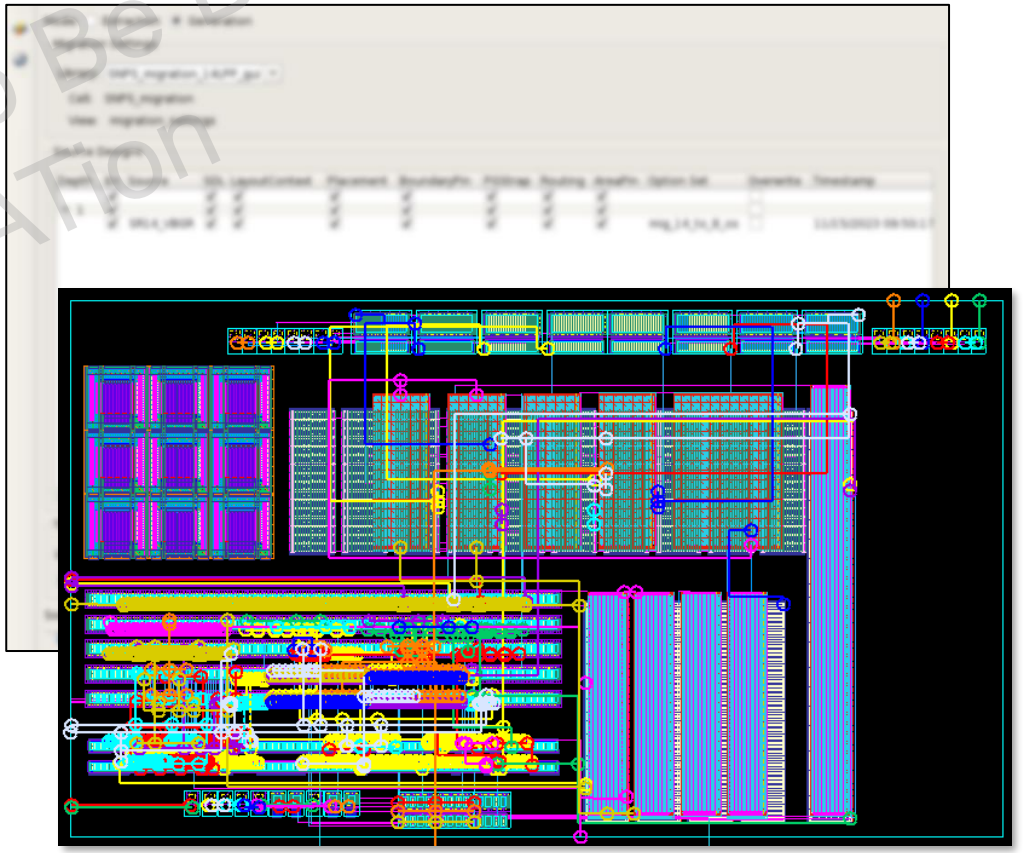
Custom Compiler Design Platform

ASO.ai: Analog Design Migration Solution

Source Design: Extraction → **Constraints** → **Target Design: Generation**



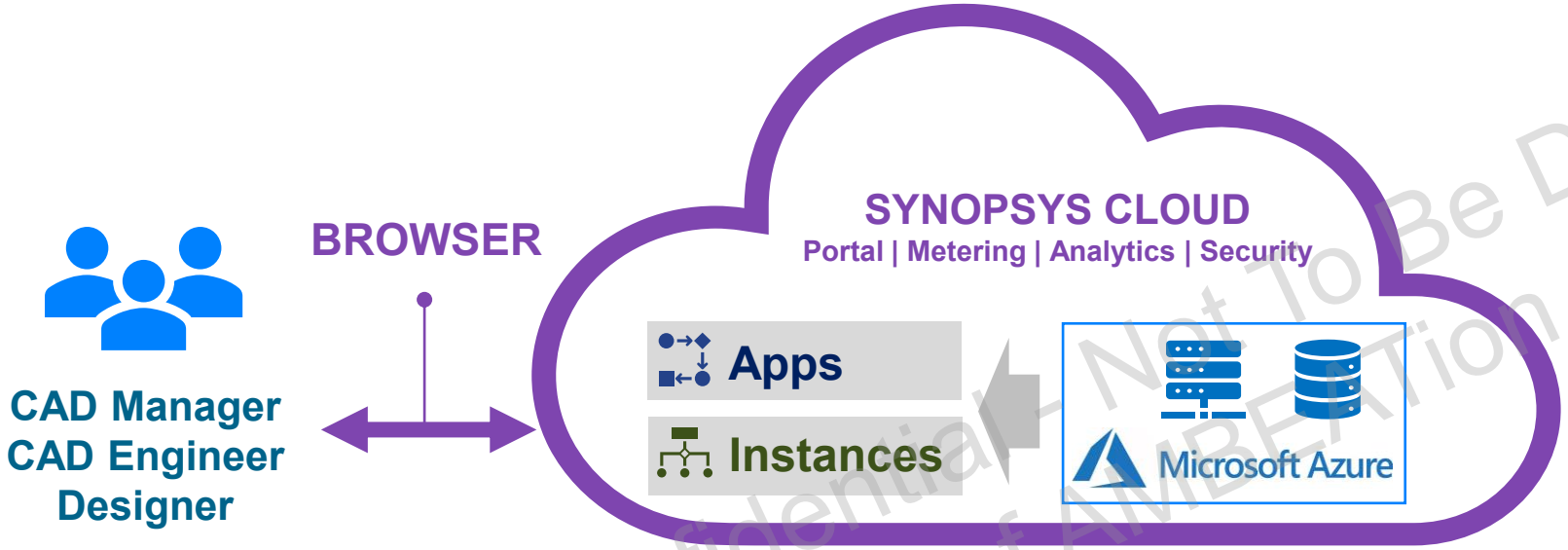




Cloud Solutions

SaaS: Software as a Service

ALL-IN-ONE BROWSER BASED EXPERIENCE



- **Optimized Compute**, **Standardized Flows**
- User and Project Management
- Provision Clusters and Schedule Jobs
- Pay-Per-Use and/or fixed term Cloud Subscription Licenses

APPS (point tools)

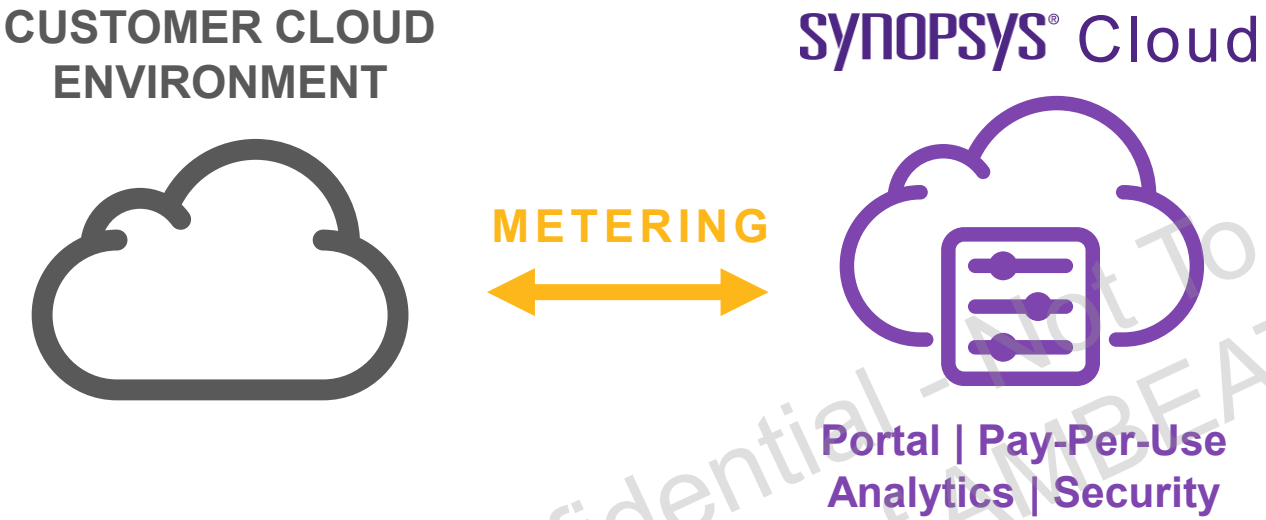
- Verification
- Timing Analysis
- Physical Verification
- Library Characterization
- Custom & Memory Verification (+ GPU!)

INSTANCES
(end-to-end flows)

- Analog Instance
- Digital Instance
- Verification Instance
- Photonic Instance

BYOC: Bring Your Own Cloud

Simplified use model



FlexEDA with Unlimited **Pay-Per-Use** (PPU) Access:

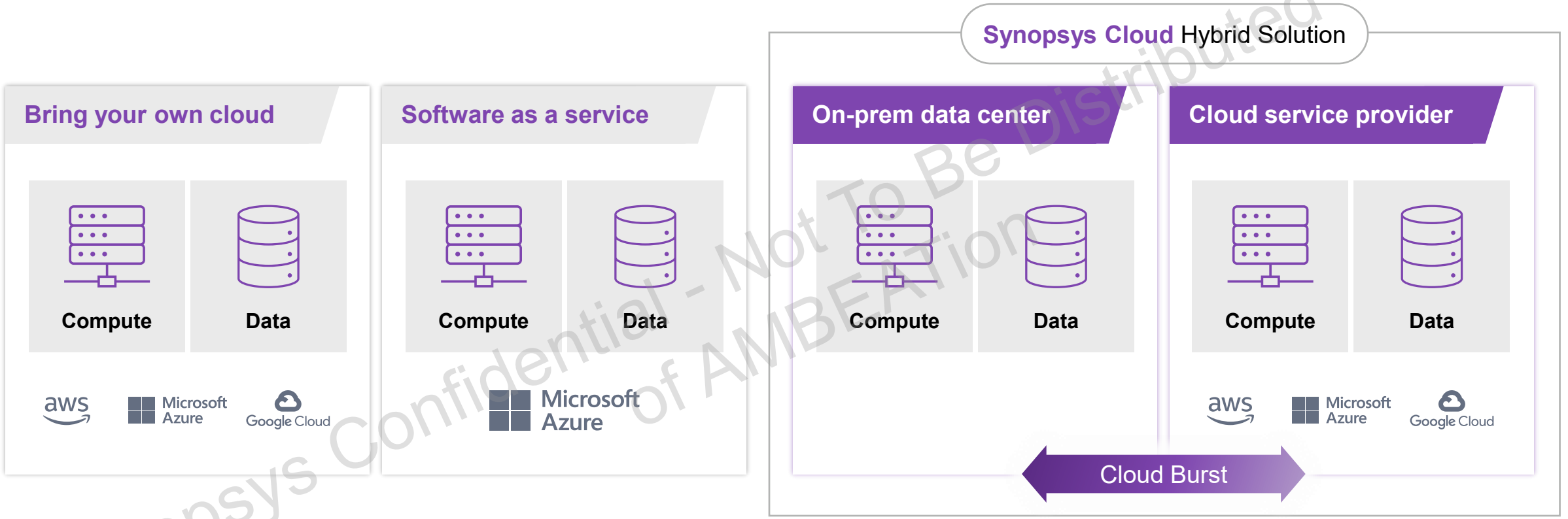
- Same use model with any choice of third-party cloud
- No license servers to manage for PPU tools
  - VCS/VIP, PrimeTime, IC Validator, PrimeSim
  - PrimeLib, StarRC, VC Formal, PrimeSim Reliability

Azure

aws

Google Cloud Platform

Comprehensive Cloud Scaling



Up to 40%
faster time to results

Up to 50%
productivity improvement

SYNOPSYS®

Thank you

For any questions Marco.Inglardi@synopsys.com