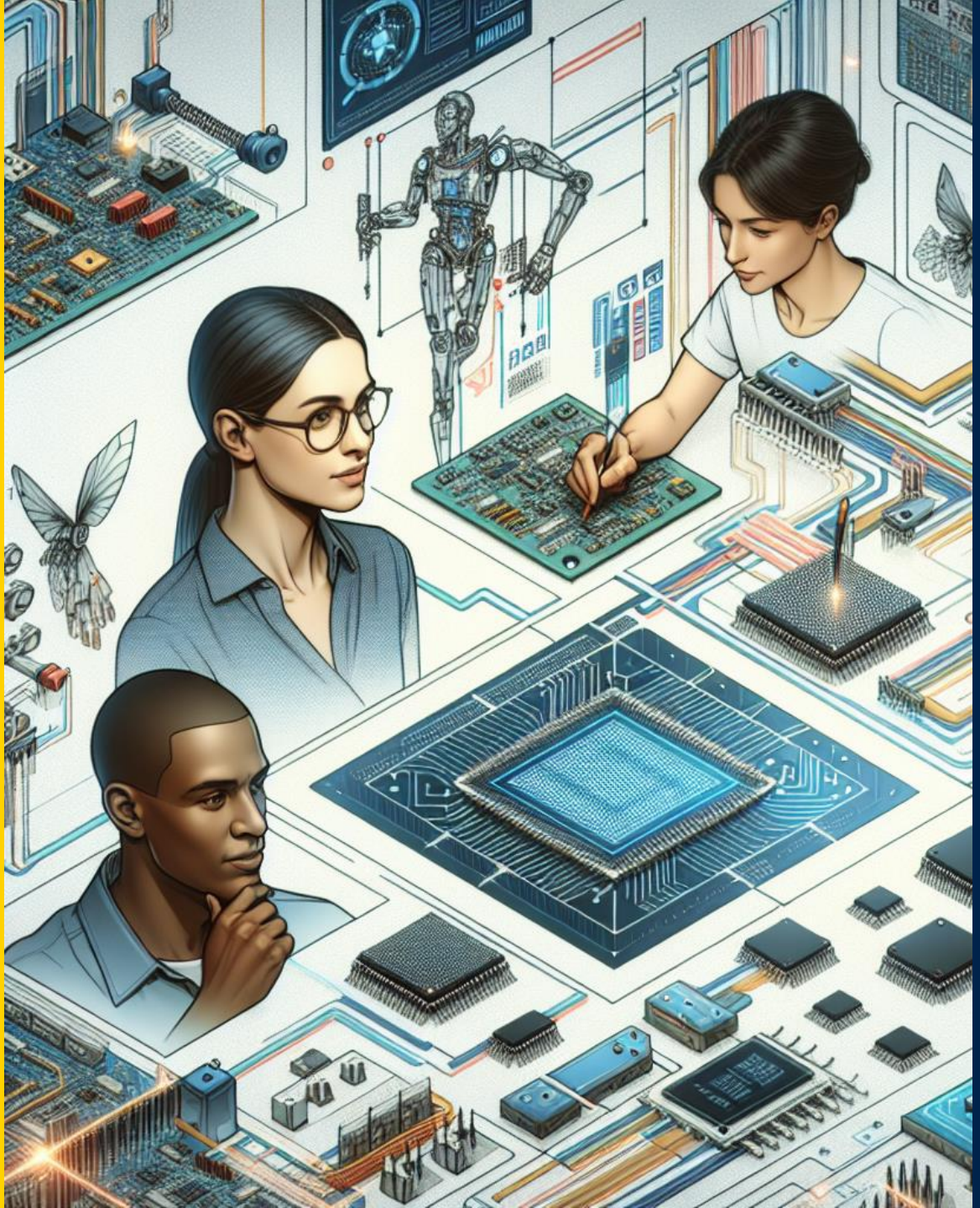


A Follow-up to the AMBEATion Project

Dalibor BARRI, Patrik VACULA, Jiri JAKOVENKO, Vladimir JANICEK

STMicroelectronics, CTU-FEE

21 July 2025

Collaboration

Academic: CTU, NTHU, NCU, NTUST, Taiwan Tech

- Taiwan universities
  - National Tsing Hua University (NTHU):
    - Renowned for semiconductor research, AI, and ML
  - National Central University (NCU):
    - Strong in semiconductor technology and EDA
  - National Taiwan University of Science and Technology (NTUST, Taiwan Tech):
    - Focus on practical and applied research in semiconductor design
- European Universities:
  - Czech Technical University (CTU):
    - Leading in electrical engineering, AMS design, and automation

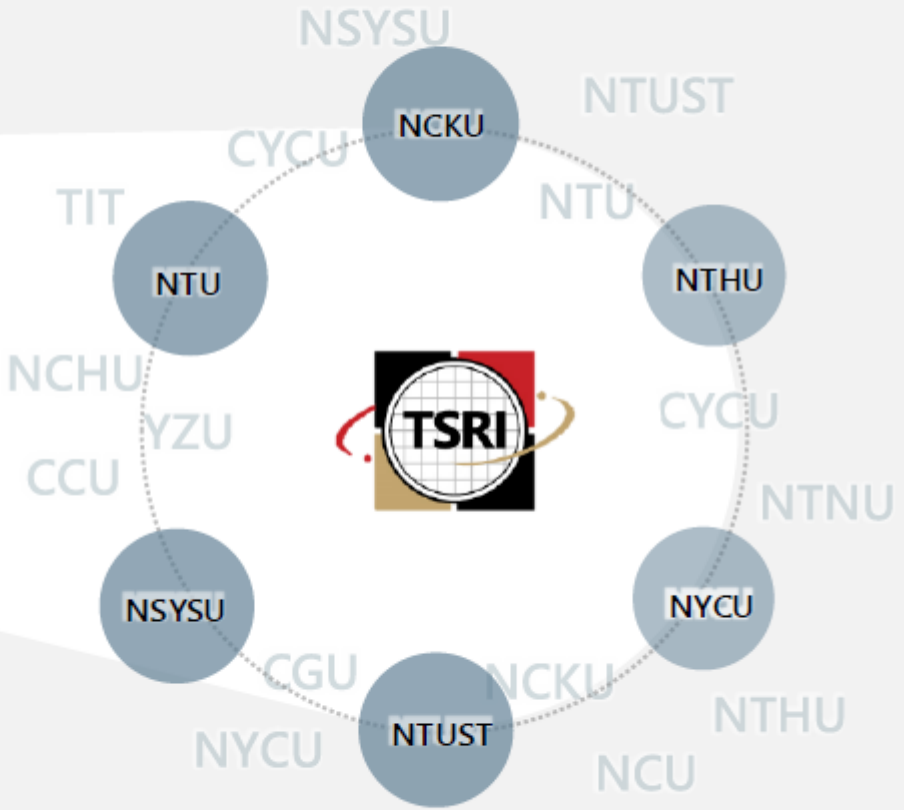
Industry: STMicroelectronics, MicroIP

- STMicroelectronics (STM):
  - Global Leader: One of the world's leading semiconductor companies
  - Expertise: Specializes in electronic components for Smart Systems
- MicroIP:
  - Specialization: Leading Taiwanese company specializing in semiconductor IP and EDA tools
  - Innovation: Known for developing innovative solutions for semiconductor design automation
  - Industry Connections: Strong industry connections that ensure the project's methodologies are robust and commercially viable

Taiwan's Talent Cultivation Ecosystem

TSRI's Proven Model

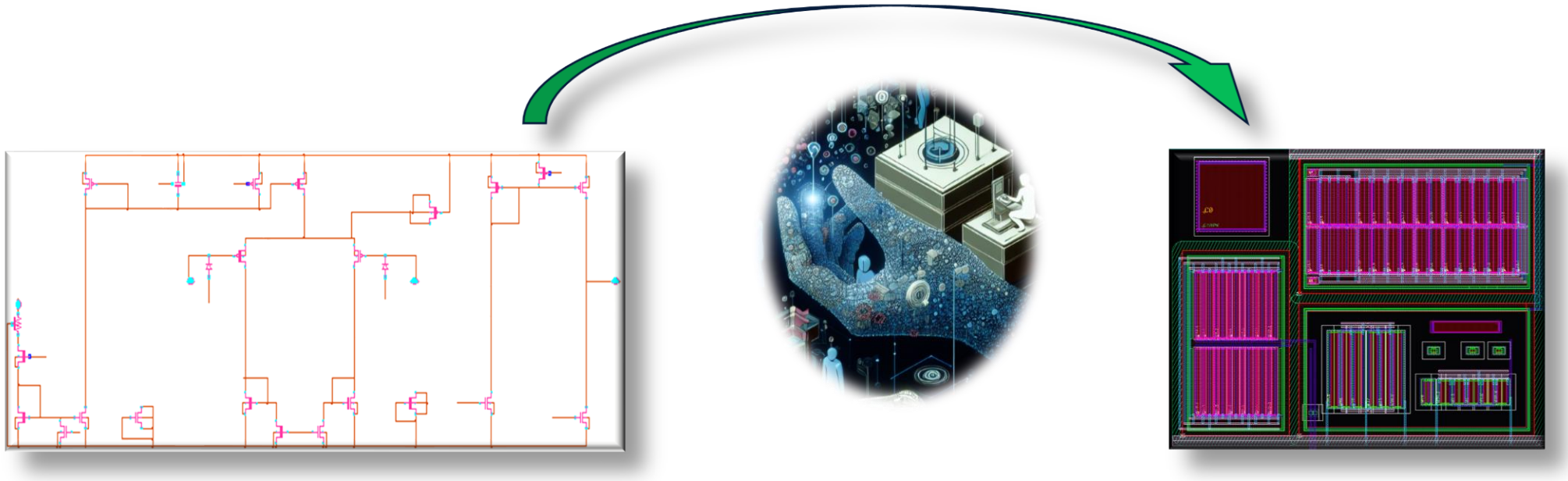
NARLabs National Applied Research Laboratories
Taiwan Semiconductor Research Institute



Work with +50 universities
and +600 research groups

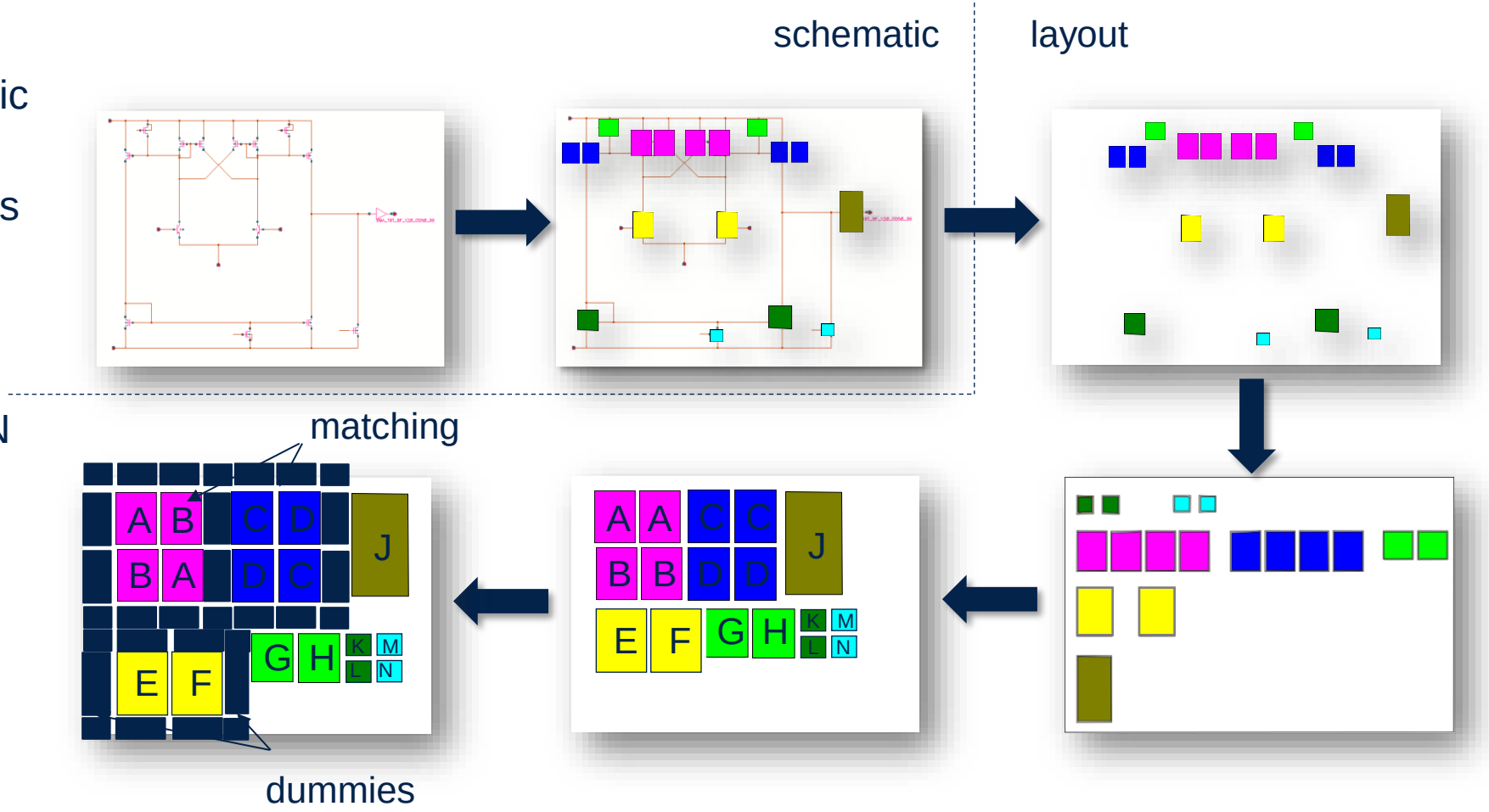
Introduction

- **Title:** Analog Layout Design Automation Project
- **Aim:** Revolutionize analog-mixed-signal (AMS) integrated circuit (IC) design using machine learning (ML) and artificial intelligence (AI).



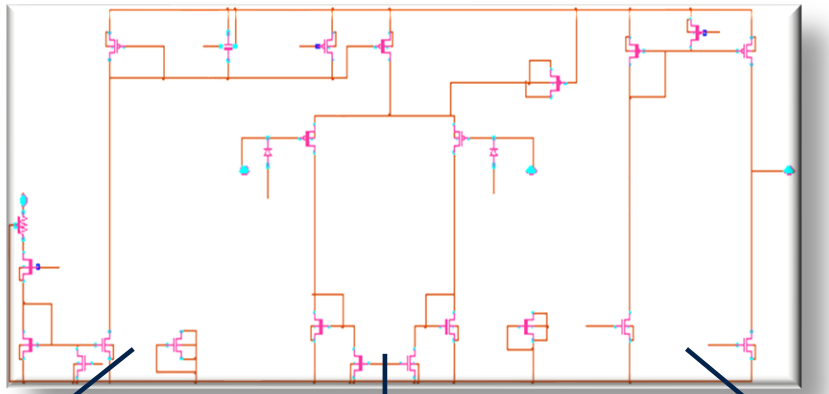
Objectives

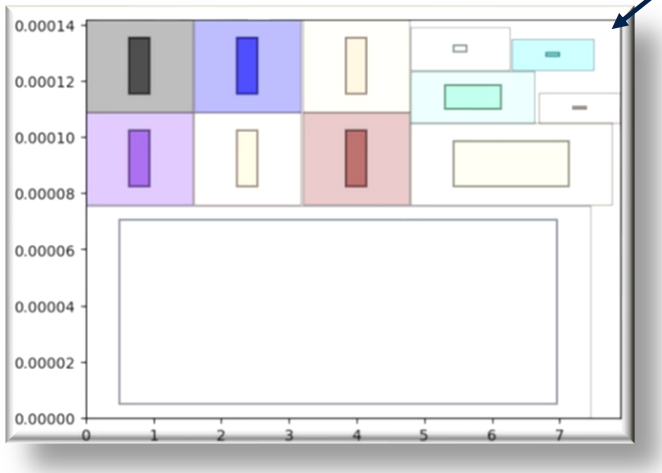
- **Objectives:**
  - Develop tools for automatic constraint generation
  - Create abstract generators for AMS IC placement
  - Develop a 2D AMS IC auto-placer
  - To realize matching by NN
  - To respect LDE effects
  - Support hierarchical databases
  - Create basic routing between topologies and devices



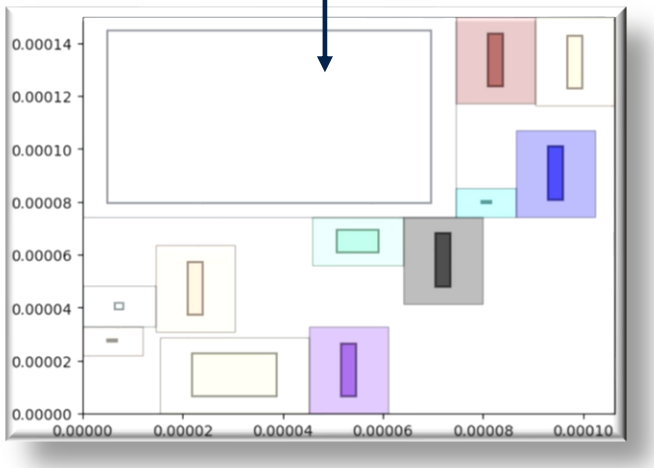
State of the Art

- Nowdays results
  - AMBEATion project
  - MAGICAL project
  - ALIGN project...

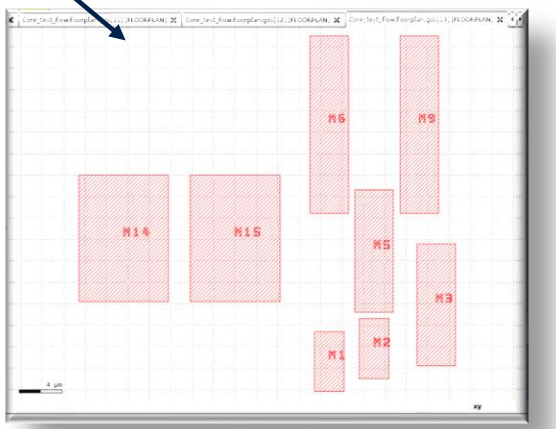




rectangular



NLP



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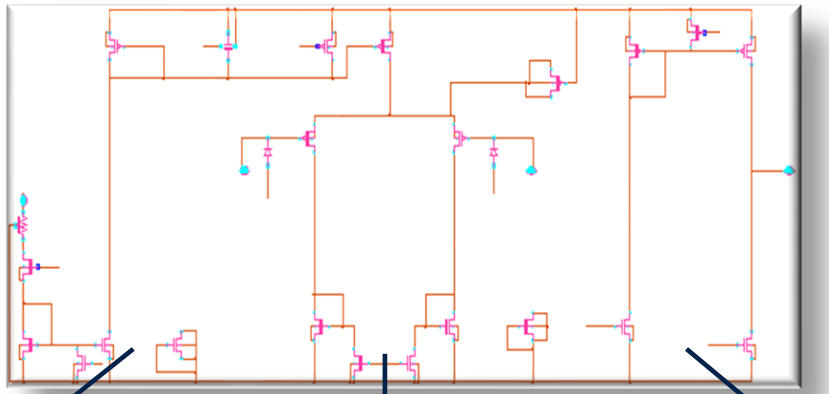

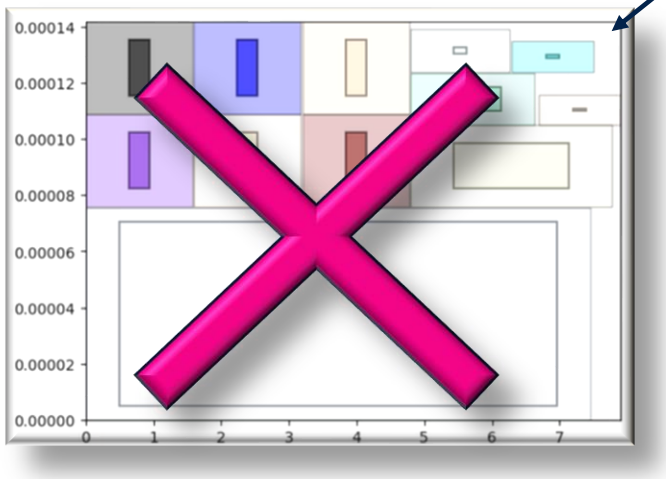

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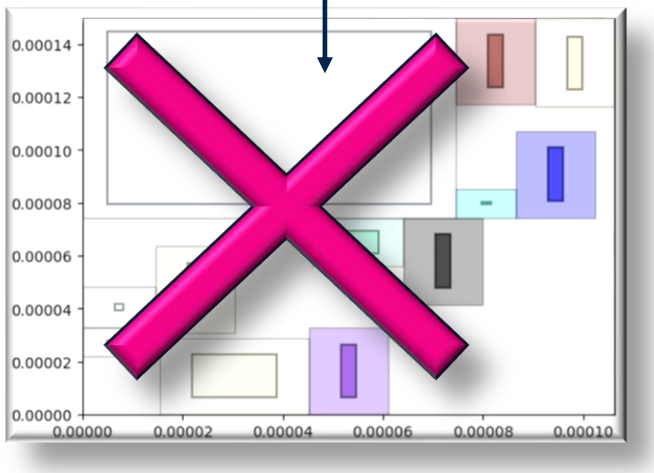

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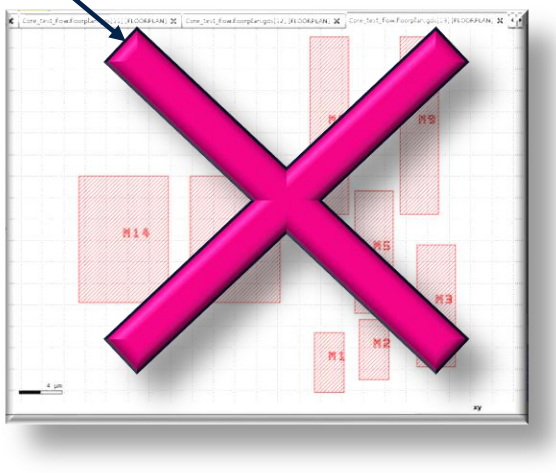

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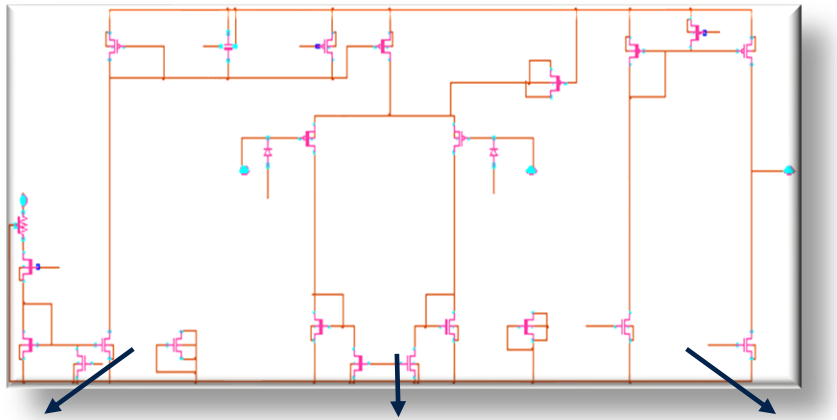
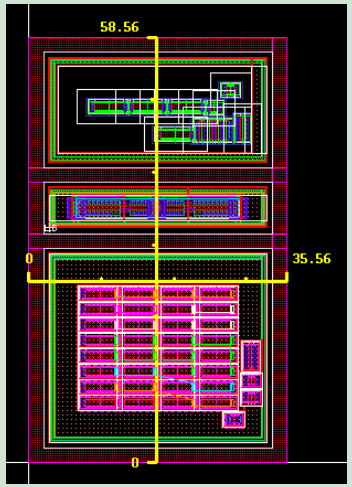
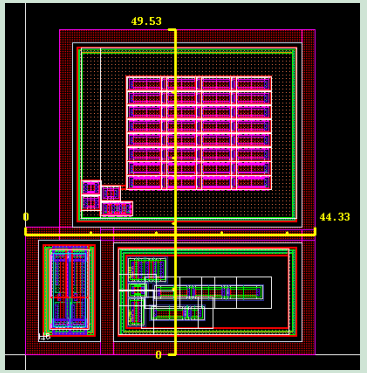
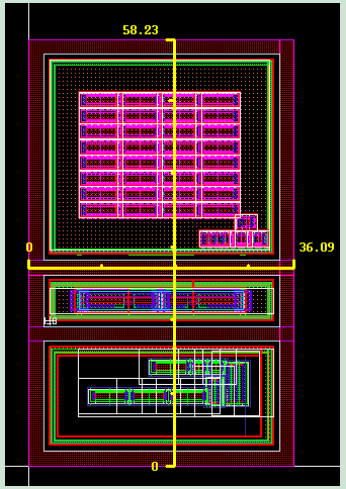


Preferred Area	Preferred Connection	Compromise
A = 2 083um² P2P = 0.295 T = 0.44s	A = 2 196um² **P2P = 0.068** T = 5min	A = 2 102um² P2P = 0.084 T = 4.44s







IC Flow

Specification and Requirements

Define the specifications and requirements of the analog circuit.

Gather all necessary design documents and constraints.

Schematic Design

Create the schematic diagram of the analog circuit.

Perform initial simulations to verify the functionality.

Pre-Layout Simulation

Run detailed simulations to ensure the design meets the specifications.

Make necessary adjustments to the schematic based on simulation results.

Floorplanning

Plan the layout of the circuit, considering the placement of major components.

Optimize the layout for performance, area, and power consumption.

Placement

Place the individual components (transistors, resistors, capacitors, etc.) on the layout.

Ensure proper spacing and alignment according to design rules.

Routing

Connect the components with metal interconnects.

Ensure minimal parasitic resistance and capacitance.

Layout Verification

Perform Design Rule Check (DRC) to ensure the layout adheres to manufacturing constraints.

Conduct Layout Versus Schematic (LVS) check to ensure the layout matches the schematic.

Post-Layout Simulation

Extract parasitics from the layout.

Run post-layout simulations to verify the performance with parasitics included.

Layout Optimization

Make necessary adjustments to the layout based on post-layout simulation results.

Iterate the process of placement, routing, and verification as needed.

Final Verification

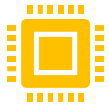
Perform final DRC and LVS checks.

Conduct additional checks such as Antenna Check, Electromigration Check, etc.

Tape-Out

Prepare the final layout for manufacturing.

Generate the necessary files (GDSII, OASIS) for fabrication.



Fabrication

Send the design to the foundry for manufacturing.

Monitor the fabrication process and address any issues that arise.

Testing and Validation

Test the fabricated ICs to ensure they meet the design specifications.

Validate the performance and functionality of the ICs.

IC Flow

AMBEATion

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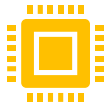

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IC Flow

AMBEATion

Follow-up activities

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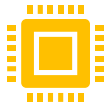

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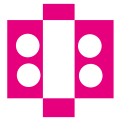
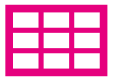
Placer Classification

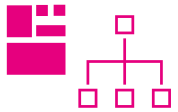


(**L0**) Level 0 placers : Abstract generators

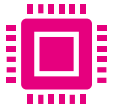


(**L1**) Level 1 placers: Regular Structure Placers

(**L2**) Level 2 placers: IP level Placers



(L3) Level 3 placers: Top Level Placers (Floorplaning)



(L4) Level 4 placers: Package Placers

(L5) Level 5 placers: Chip-lets Placers

L0 Placer: Abstract generators

- it means pCell representation (in another word how instances are represented in layout by area – instance area)

L1 Placer: Regular Structure Placers

- Regular and sensitive structure placement (current mirror, differential pair, resistor ladder…)
- Matching is required.
- Logical structure

L2 Placer: IP level Placers

- Placement of the instances on the IP level (it means placement of the instances generated in L1 level and the rest of the instances on that IP level)
- As IP level can be understood OpAmp, ADC, bias, BGP …

L3 Placer: Top Level Placers – Floorplanning

- Placement of the IPs on the upper level (it means placement BIAS, OpAmp, ADC,… on the dedicated level)

L4 Placer: Package Placers

- Optimize pad and solder ball position

L5 Placer: Chip-lets Placers

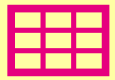
- Optimize interconnection between chips (through silicon via position, ball position optimization – WLCSP package)

Placer Classification

AMBEATion

Follow-up activities

(**L0**) Level 0 placers : Abstract generators



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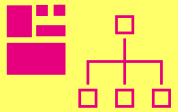

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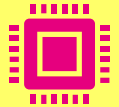

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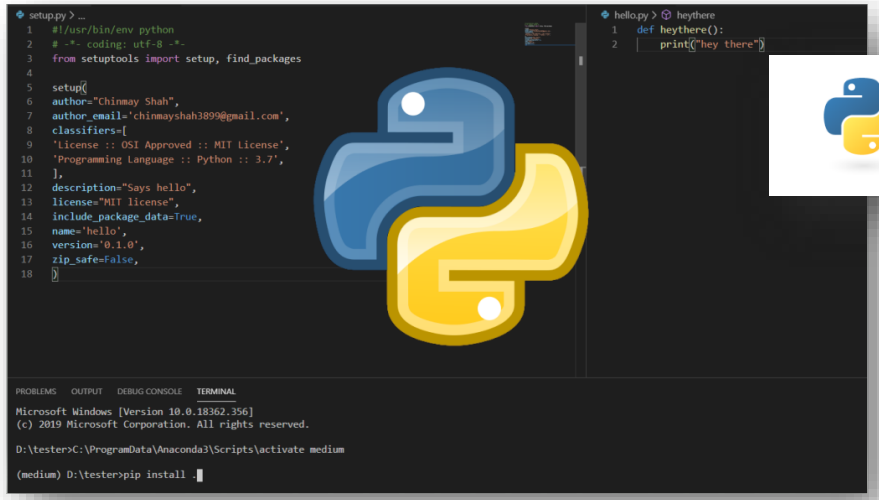
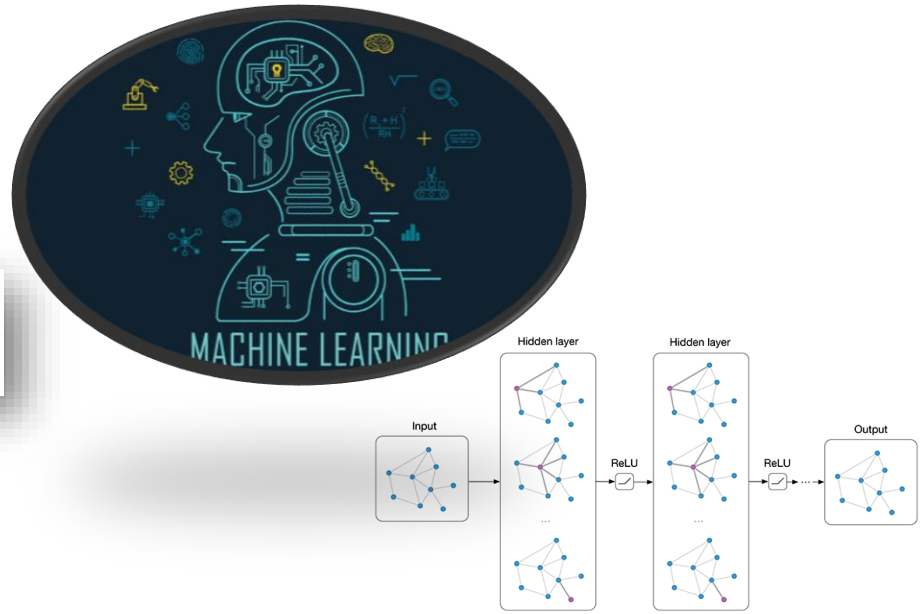
SW to be used in the follow up project



python™

SYNOPSYS®



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Summary

Summary:

Today, it has been presented the key goals, achievements, and ongoing developments of the **AMBEATion** project and its follow up project activities.
It was highlighted how this initiative is transforming analog-mixed-signal (AMS) IC design through advanced machine learning and artificial intelligence techniques.
The comprehensive design flow, placer classification, and strong collaboration between academia and industry were also discussed.

The **follow up activities** are focused on developing:

- new **placer** started from knowledge given from previous projects (like AMBEATion project is)
- **routing** procedure to do interconnection for L1, L2 and L3 placement levels
- **matching** pattern by NN

Thank you

- to EU for supporting to develop AMBEATion project
- to all project partners
- to project Leader (Daniele Jahier Pagliari)

Our technology starts with You

Find out more at www.st.com