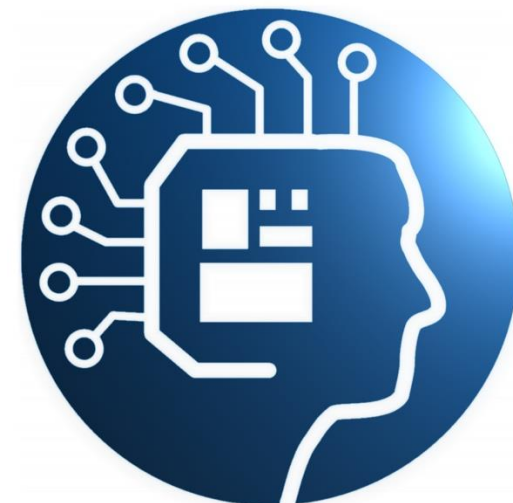
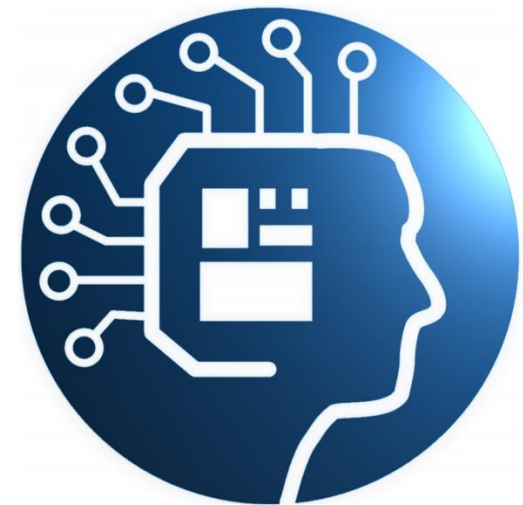


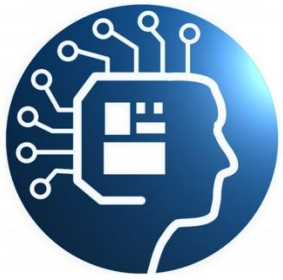
Welcome Note

Daniele Jahier Pagliari, Politecnico di Torino
daniele.jahier@polito.it



Meeting Agenda



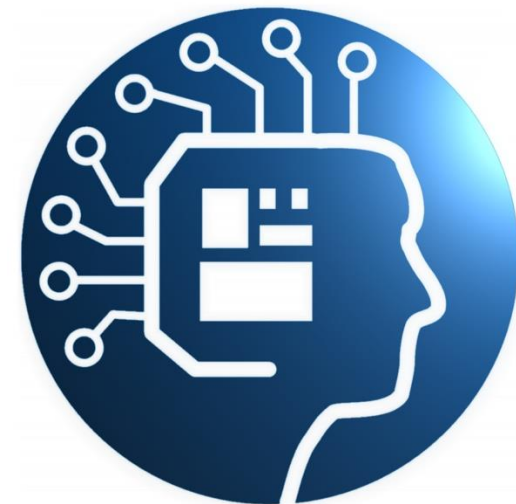


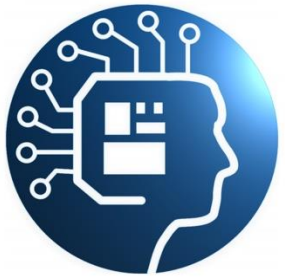
Meeting Agenda

Start Time	Title	Speaker
15:00	Welcome Note – Lessons Learned from the AMBEATion Project	Daniele Jahier Pagliari Politecnico di Torino
15:20	Effective Analog ICs Floorplanning with Relational Graph Neural Networks and Reinforcement Learning	Davide Basso University of Trieste
15:40	Learning to Act like a Pro: Discovering Procedural Models of Expert Workflows for Assistance and Validation	Antonino Furnari University of Catania
16:00	The AI Revolution in ST Design Flow	Michelangelo Grosso ST Microelectronics
16:20	A Modern Solution for Analog/Mixed-Signal Design	Marco Inglardi Synopsys
16:40	A Follow-up to the AMBEATion Project	Dalibor Barri ST Microelectronics

Lessons Learned from the AMBEATion Project

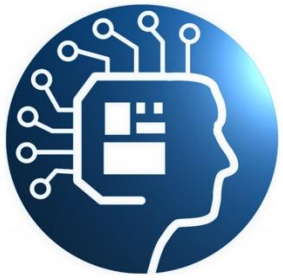
Daniele Jahier Pagliari, Politecnico di Torino
daniele.jahier@polito.it





The AMBEATion Project

- *Analog/Mixed Signal Back End Design Automation based on Machine Learning and Artificial Intelligence Techniques*
- Marie Skłodowska Curie Research and Innovation Staff Exchange Action (MSCA-RISE)
- Sep. 1st 2021 – Aug. 31st 2025



AMBEATion's Consortium



**Politecnico
di Torino**

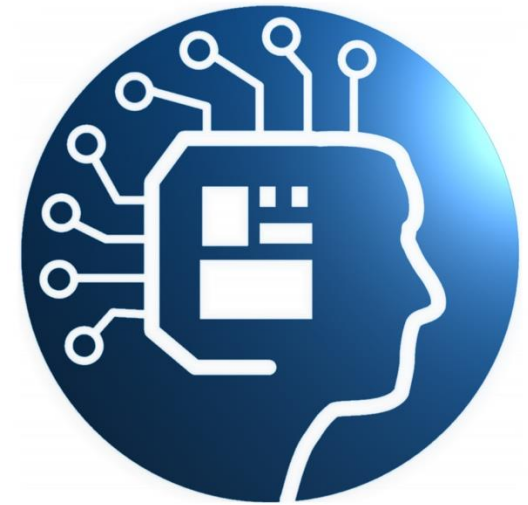


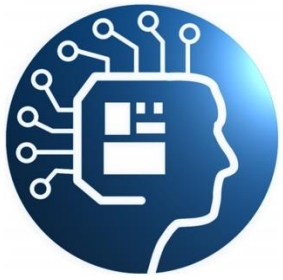
UNIVERSITÀ
degli STUDI
di CATANIA



SYNOPSYS®

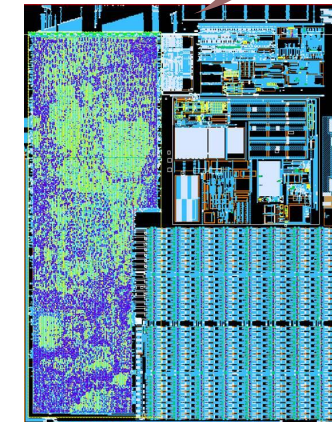
Context and Motivation

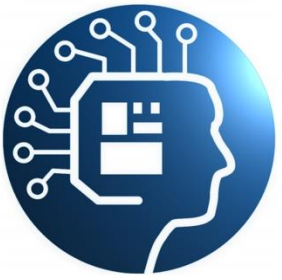




Context and Motivation

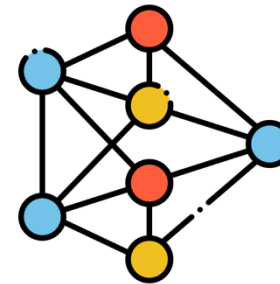
- **Analog Mixed-Signal (AMS) ICs** are pervasive:
 - Internet of Things (IoT), Smart & Autonomous Driving, Active Assisted Living (AAL)
- **Digital blocks** → computational tasks
- **Analog blocks** → power conversion, A/D and D/A conversion, actuation, thermal/voltage/current sensing, signal conditioning, etc.



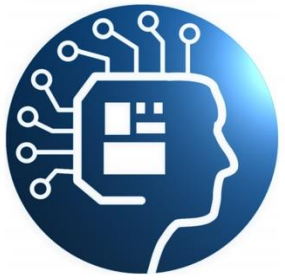


Context and Motivation

- Digital EDA tools have achieved remarkable levels of back-end automation.
- Analog (and thus AMS) back-end, instead, is still mostly done **manually** by experienced designers.
 - Sensitivity to Well Proximity Effect, Shallow Trench Isolation stress, thermal gradients, mismatch, process variations, etc.
 - More complex constraints: gain, bandwidth, distortion, etc, different for each class of devices.
 - No standard cells...
- Problem studied for decades. What's new?



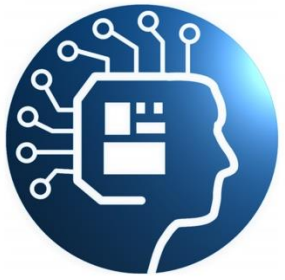
**Question: Can AI and ML help
automating AMS BE?**



State-of-the-Art

- AI and ML have been introduced in the EDA industry since several years:
 - Improve scalability, computational efficiency and QoR in different parts of the digital flow
 - A wide gap still exists within the analog domain [1]
- Some recent initiatives investigated AI/ML for AMS Back-End:
 - US DARPA IDEA Program (ALIGN Project)
 - US NSF
 - Taiwan's Ministry of Science and Technology
 - etc.

[1] B. Nikolic, "ML for analog design: Good progress, but more to do," in ACM/IEEE MLCAD, 2022



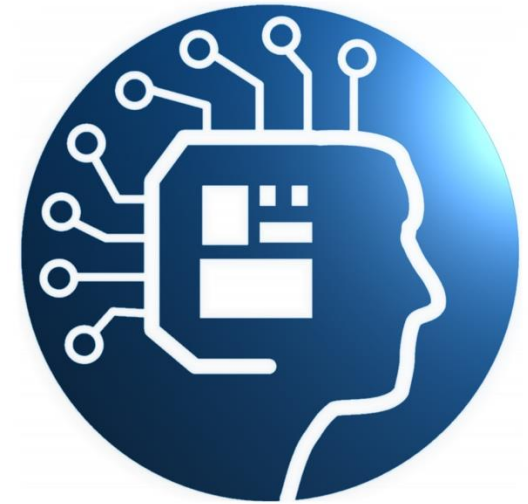
The AMBEATion Project

- **Objective**: Develop **Electronic Design Automation (EDA)** methodologies, based on AI/ML to enhance the productivity of AMS physical design
 - Increase designers' productivity → Reduce design costs
 - Mainly targeting the AMS **placement** phase.
 - Strong focus on **training, staff education and knowledge exchange** (as per MSCA goals).

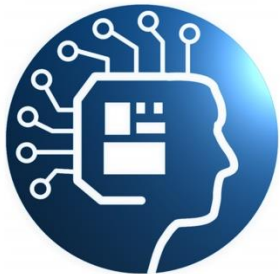
Project Website:
ambeation.polito.it



Current Status and Results

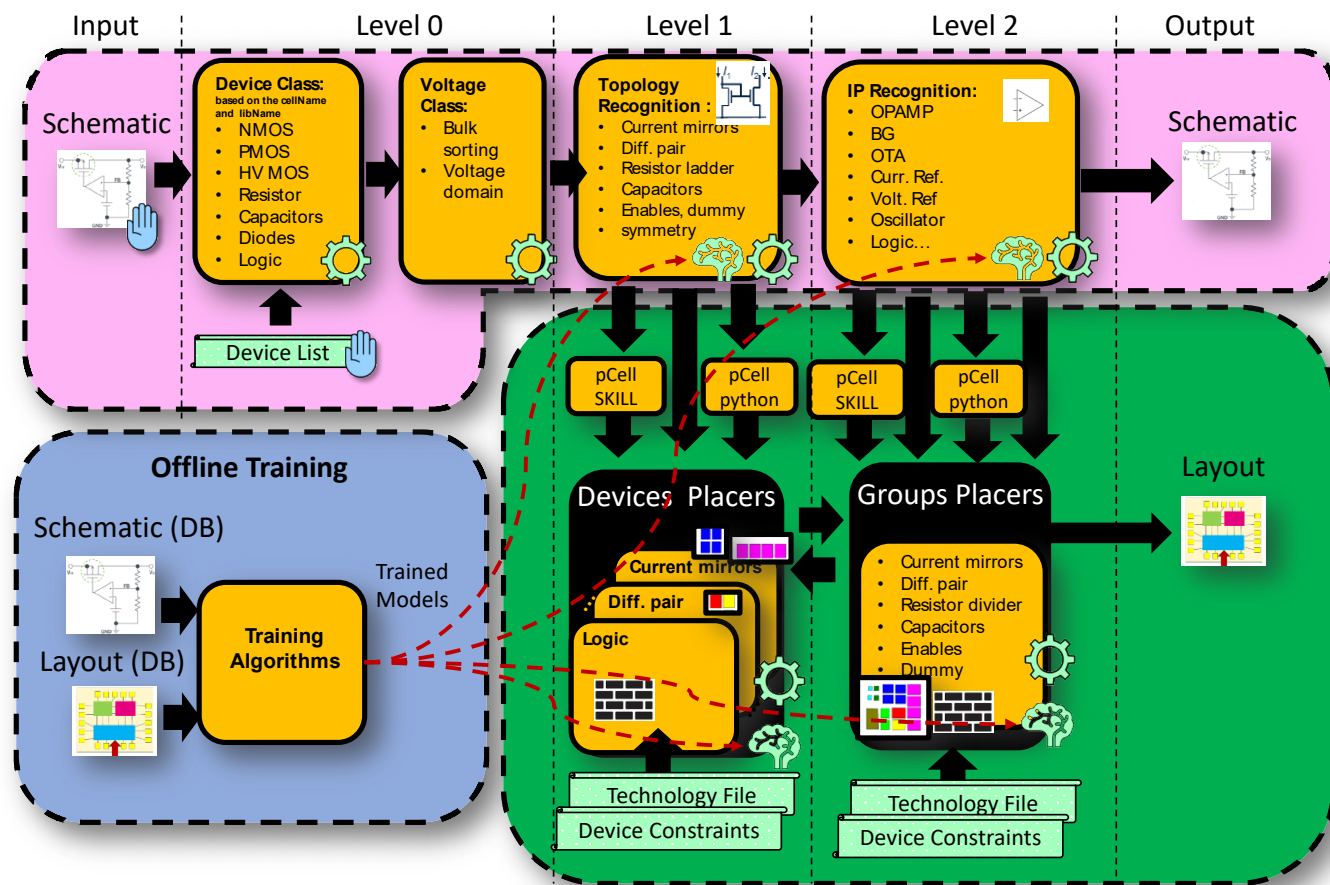


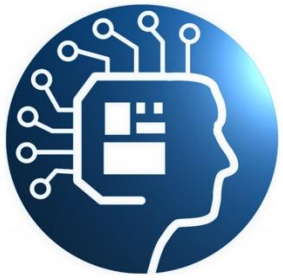
The AMBEATion project has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Skłodowska-Curie grant agreement No 101007730. Results reflect only the author's view. The Agency is not responsible for any use that may be made of them.



The AMBEATion Flow

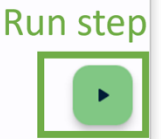
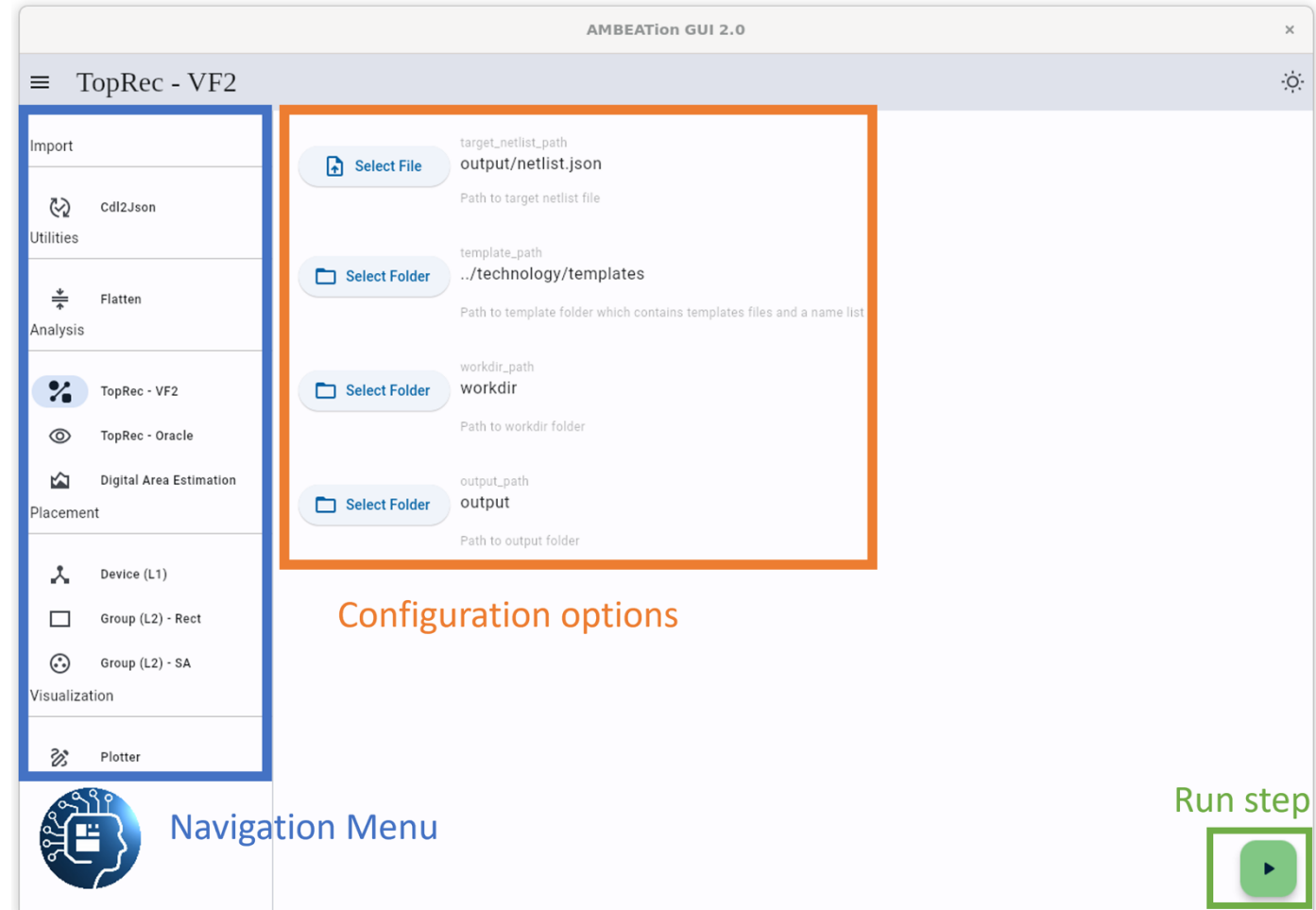
- Mix of *top-down* (digital-like) and *bottom-up* philosophies
- Two sections: **schematic** and **layout**
 - Plus offline **training** for ML
 - Organized in levels (input, device, group, etc).
- Industrial I/O formats:
 - OA, CDL, GDS-II.

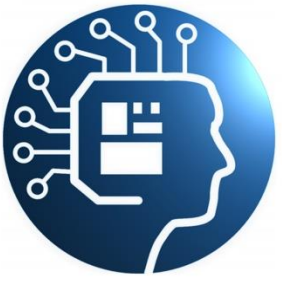




The AMBEATion Autoplacer Tool

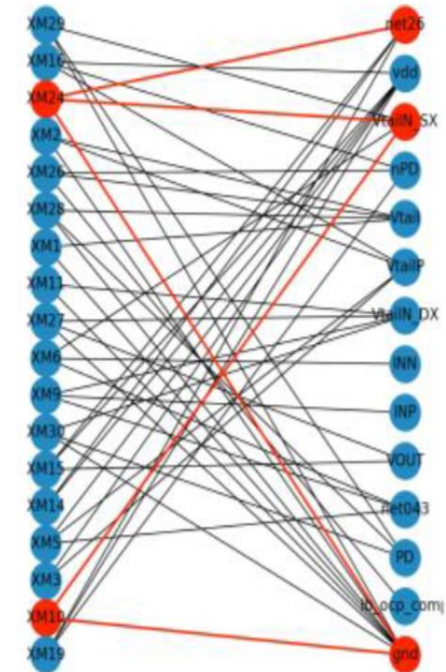
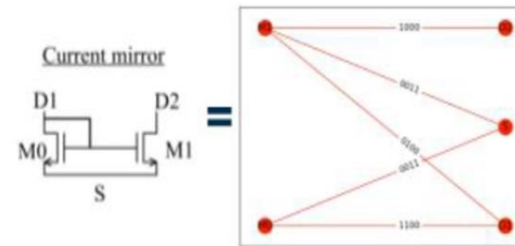
- Implementation of the flow shown in previous slides
- Entirely Python-based
- Modular interconnection of independent SW components using JSON-based internal DB files.
- Simple GUI and CLI



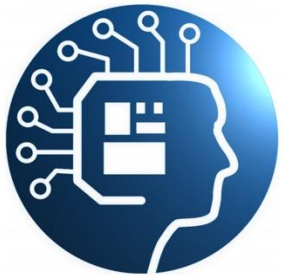


Zoom-in #1: Topology Recognition

- Find topologies (CM, DP, etc) in a bipartite graph representation of a netlist
- Classic approach: convert topology template to bipartite graph too, and apply subgraph isomorphism
 - e.g. VF2/VF3 algorithms

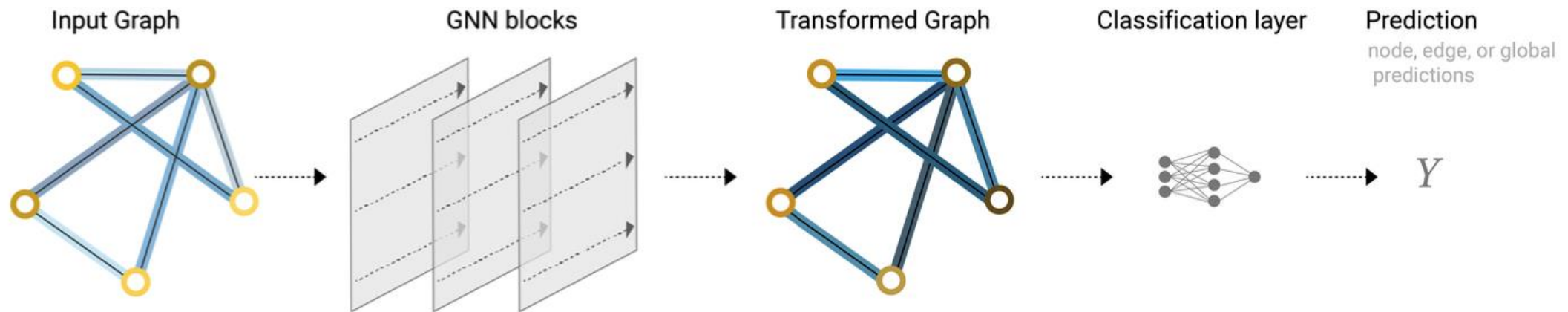


- Main limitation: ex. time for large netlists (hours/template)



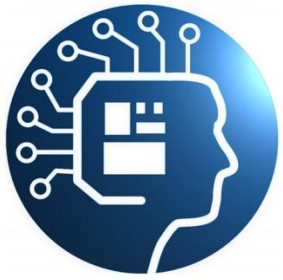
Zoom-in #1: Topology Recognition

- ML-based approach: apply Graph Neural Network (GNN) to target netlist and assign “probability of being part of a topology” to each node.



- Faster but possibly inaccurate...

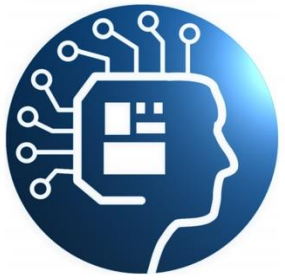
[source] <https://distill.pub/2021/gnn-intro/>



Zoom-in #1: Topology Recognition

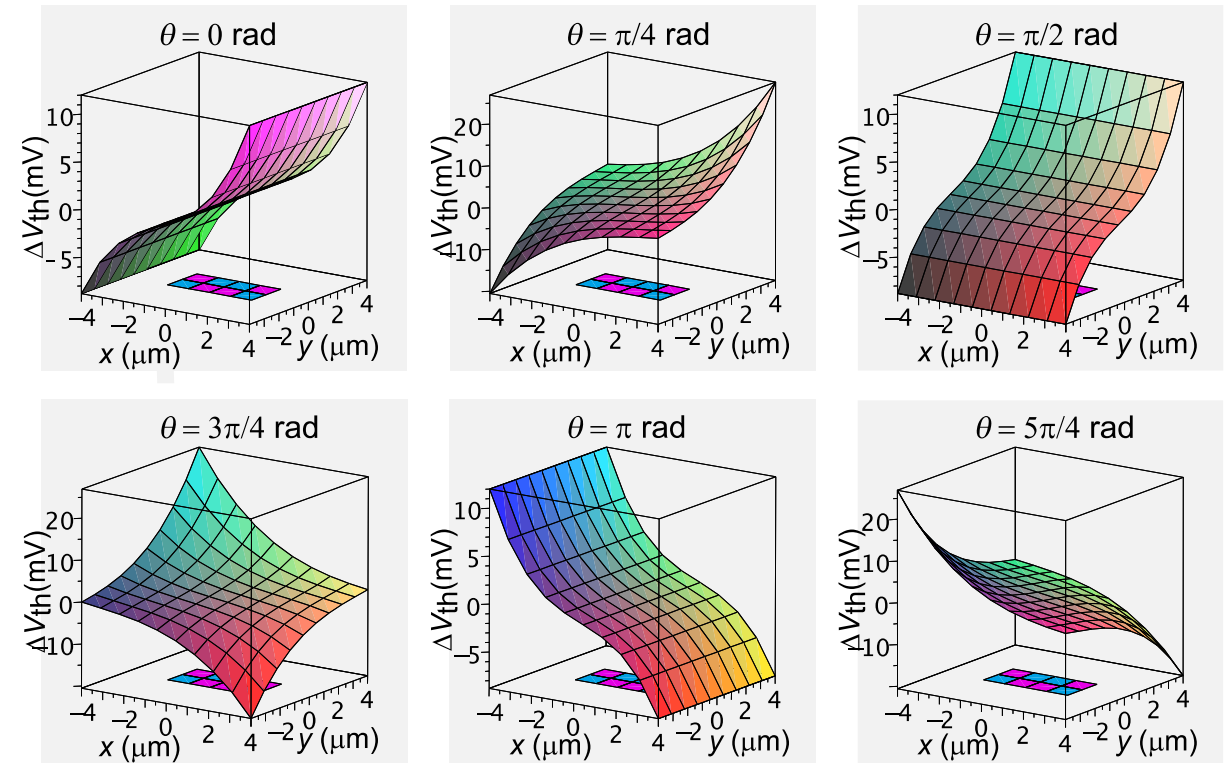
- AMBEATion's Solution:
 - Hybrid GNN + VF2 approach
 - Use GNN to quickly identify cells belonging to a topology with “high-probability”
 - Filter-out false positives with deterministic algorithm (VF2)
- Example of results (on CMs):

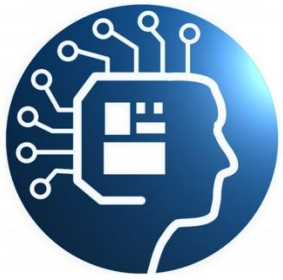
Metric	VF2	RGCN (with pre-processing)	RGCN + VF2
Accuracy	99.99%	99.48%	99.99%
Precision	96.41%	30.62%	96.62%
Recall	98.60%	99.48%	99.48%
Execution Time	10h 54min	60s	1min 57s



Zoom #2: Device Placer

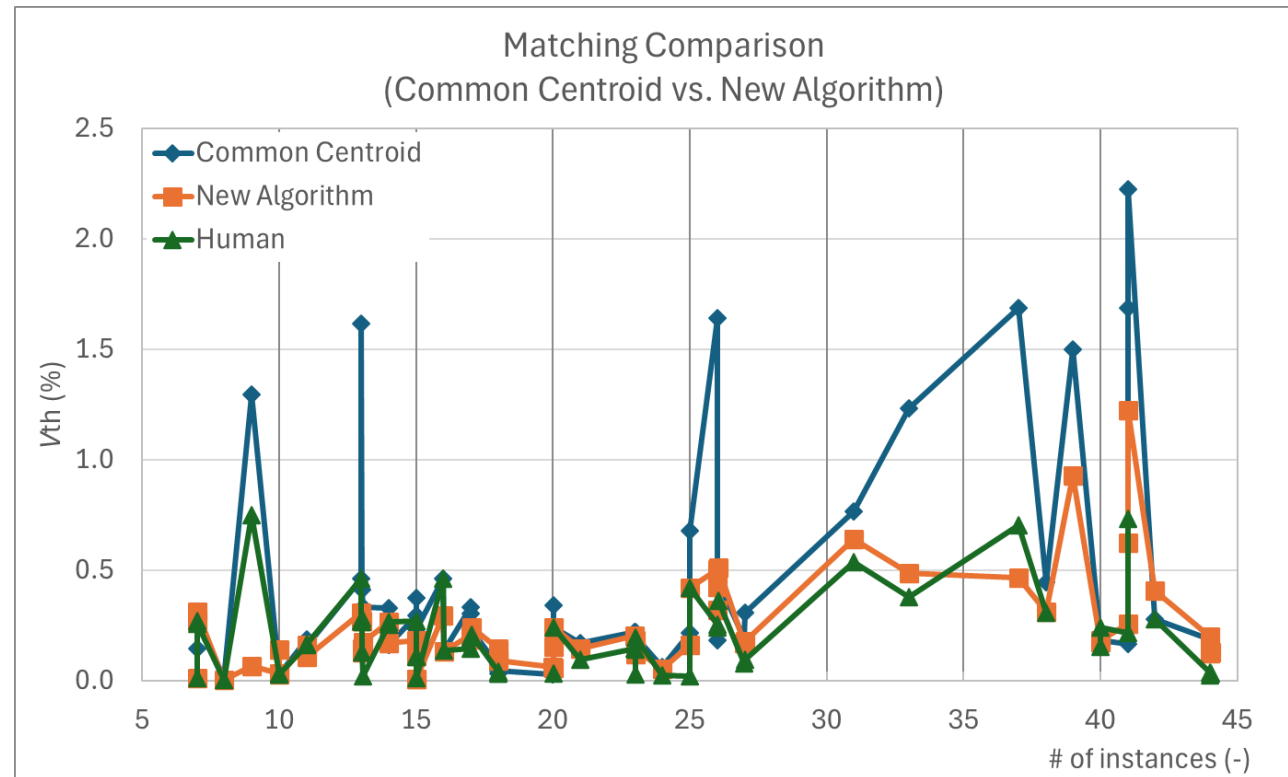
- Novel Simulated Annealing (SA)-based placement algorithm to minimize systematic device **mismatch** (due to known parasitic effects).
- Based on approximating the gradient of mismatch w.r.t. (x, y) involved devices distances as a polynomial
- Graphs: ΔV_{th} as an example of parameter influenced by mismatch

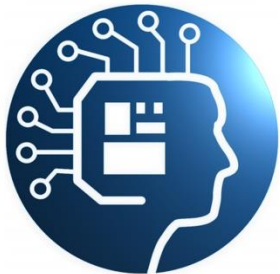




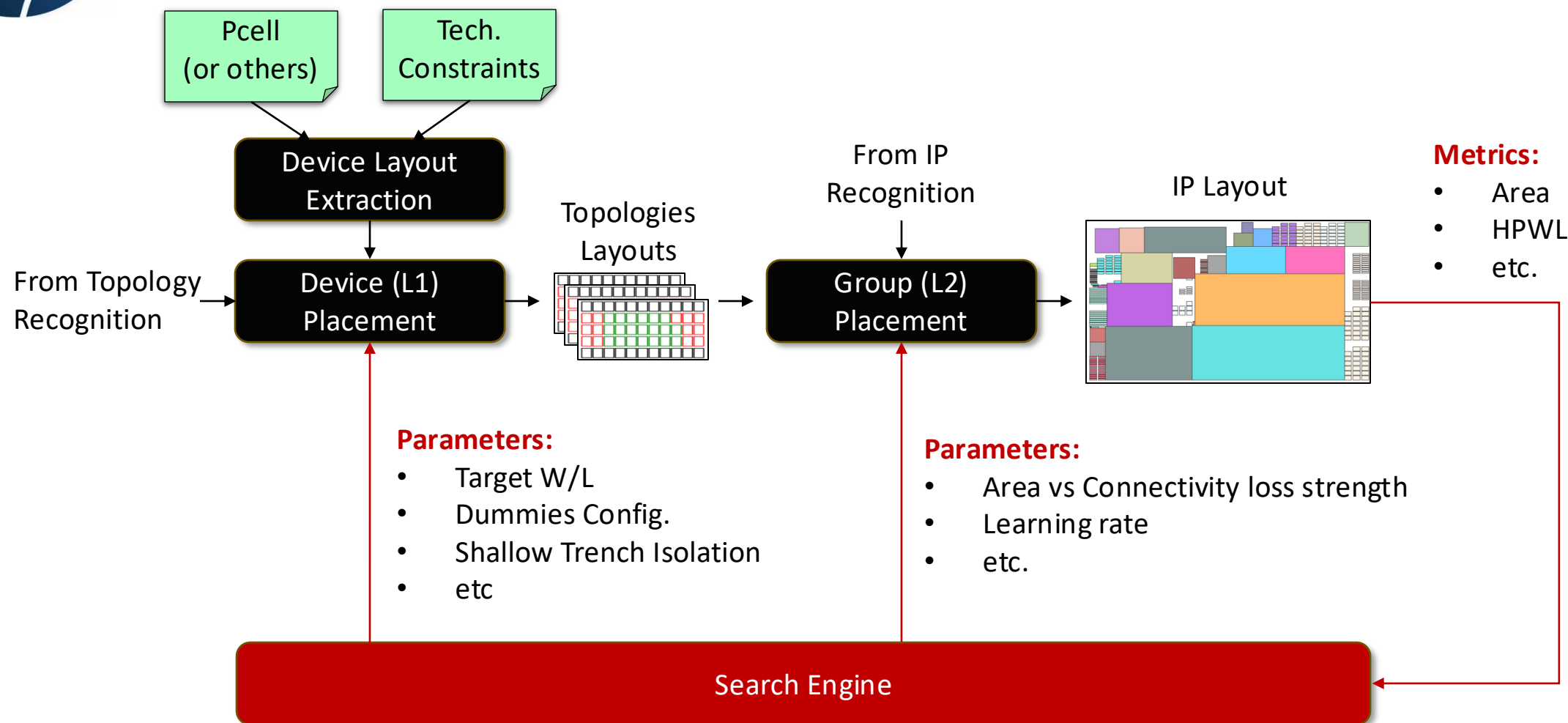
Zoom #2: Device Placer

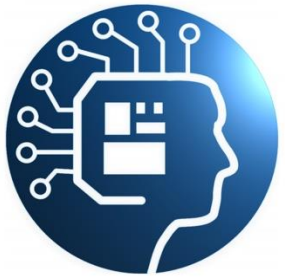
- Results consistently better than previous algorithm (Common Centroid) and often comparable with human-made layouts in terms of matching.





Zoom-in #3: Device/Group Placement





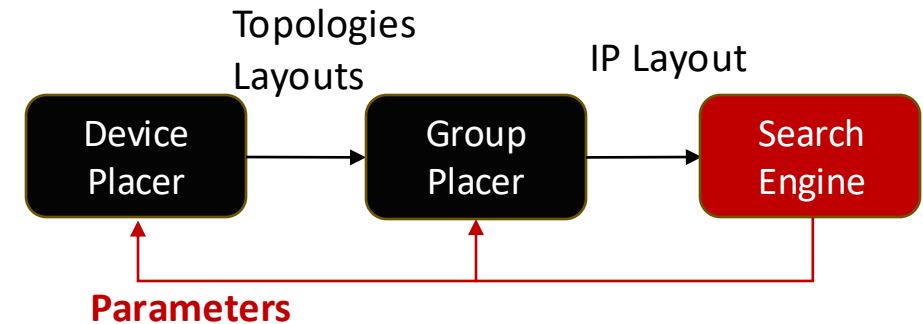
Zoom-in #3: Device/Group Placement

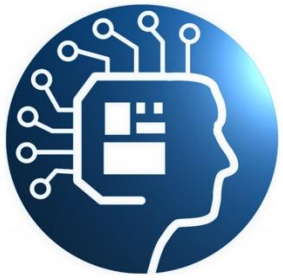
- **Alternative Group Placer Implementations:**

- Rectangle Placer (baseline)
- Simulated Annealing
- Non-Linear Programming

- **Search Engine:**

- Bayesian Optimization
- Reinforcement Learning (with NN-based reward model)



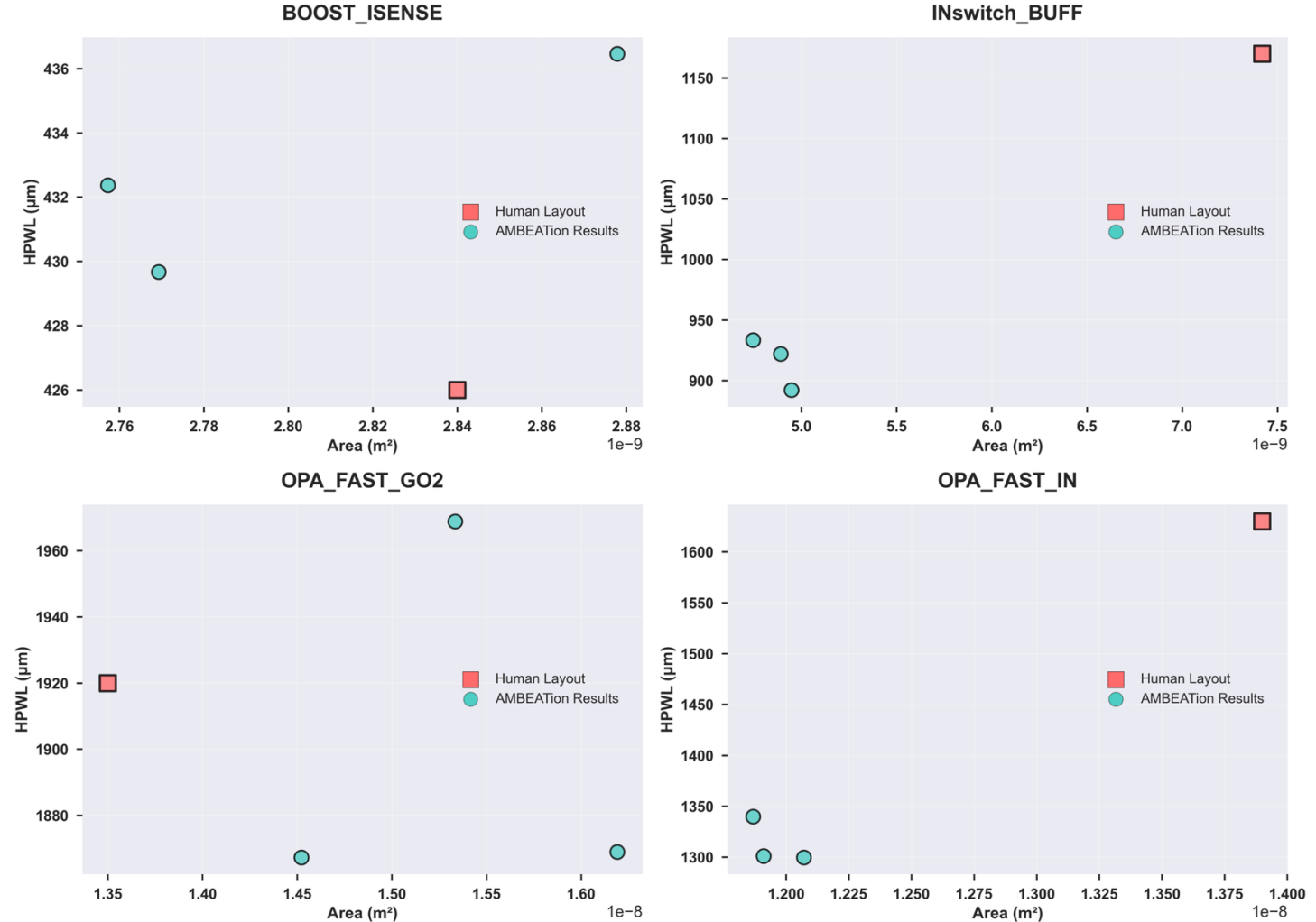


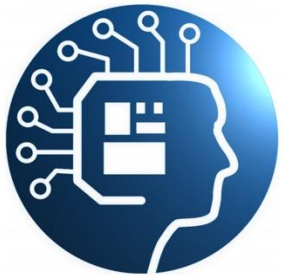
Zoom-in #3: Device/Group Placement

- Results:

- Flow outputs are **Pareto-optimal** or **dominating** human-made layout (w.r.t. the considered metrics)
- These are still relatively small circuits (200/300 devices).

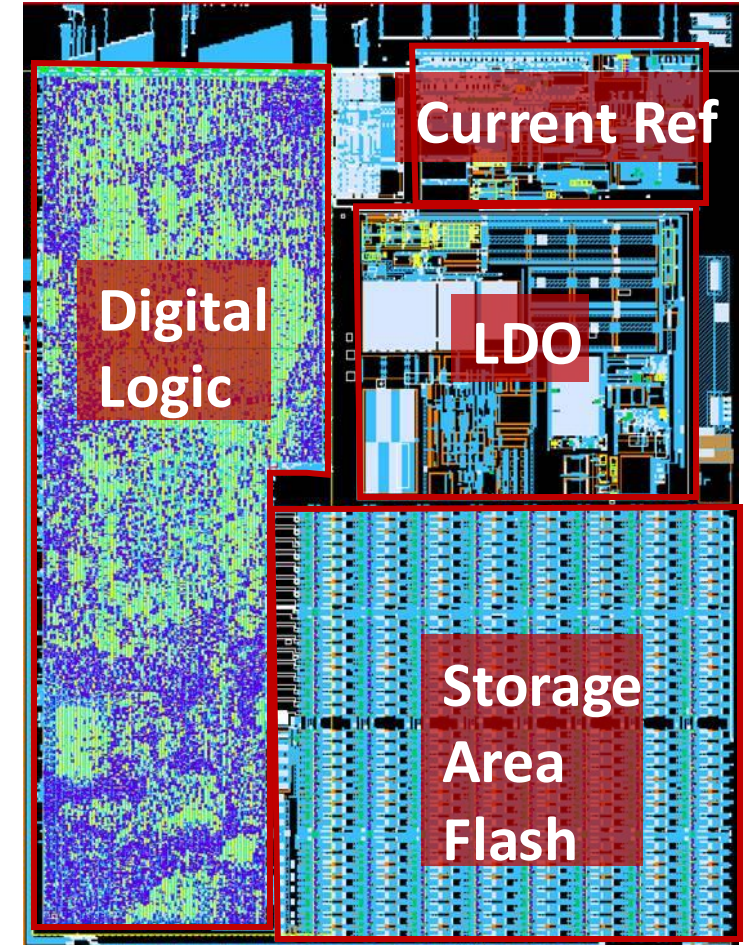
Area vs HPWL Comparison: Human Layout vs AMBEATion Results

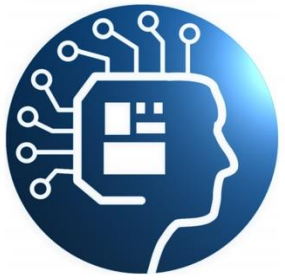




Zoom-in #4: Digital Placeability

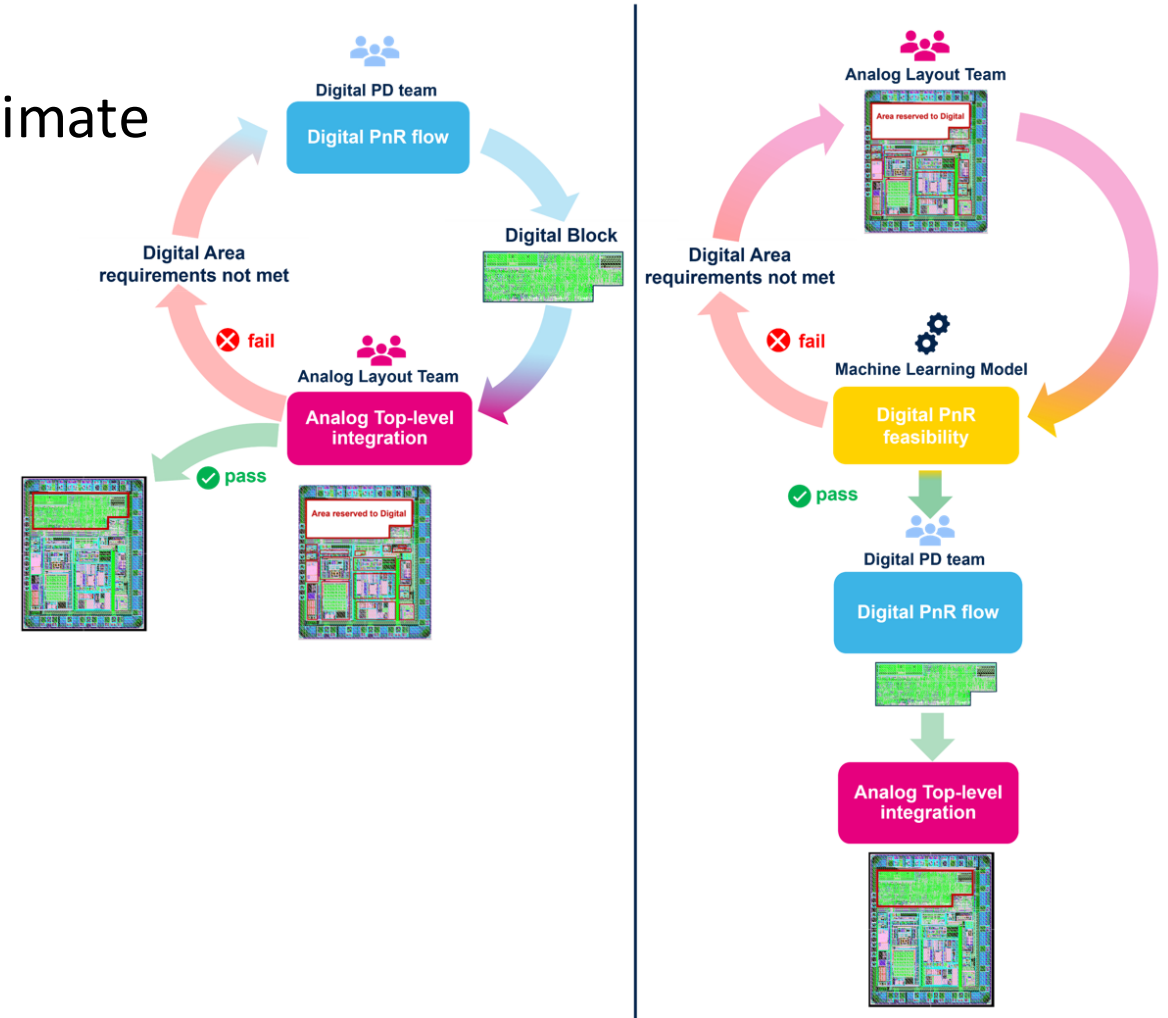
- Analog-on-top AMS ICs can contain large digital blocks:
 - Placed with SotA EDA tools in dedicated layout regions
 - Often requires multiple iterations between analog and digital teams

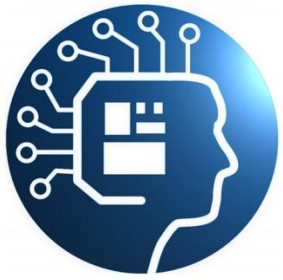




Zoom-in #4: Digital Placeability

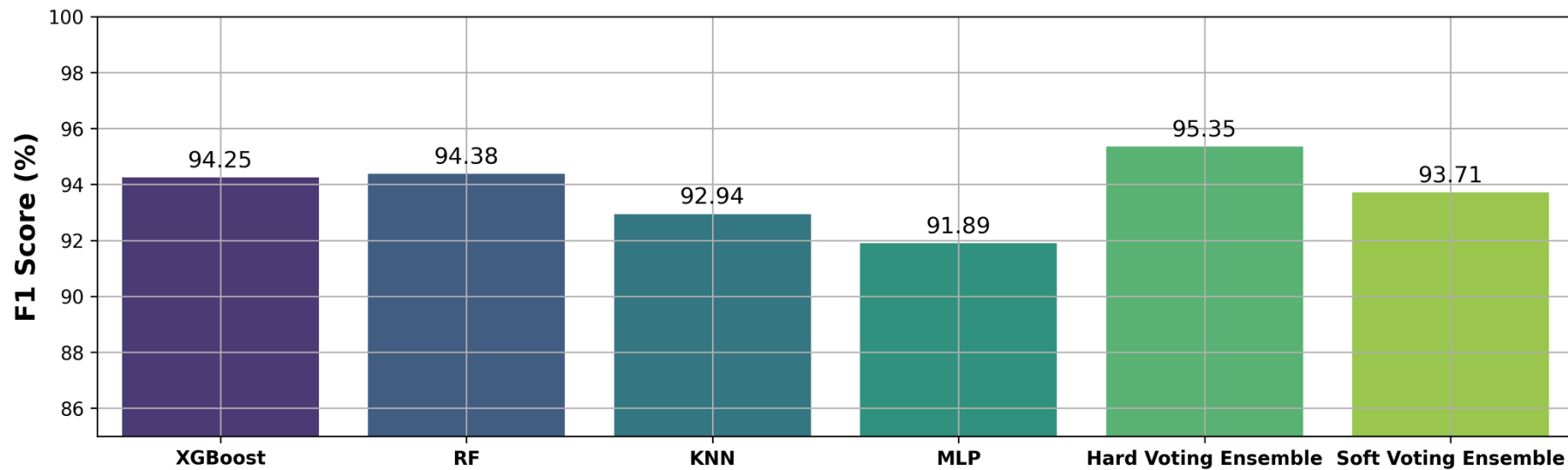
- **Proposed Approach:** Use a ML model to estimate “placeability” of digital blocks from:
 - Given layout area (and shape)
 - Simple circuit + technology features
- **Goal:** avoid costly design iterations



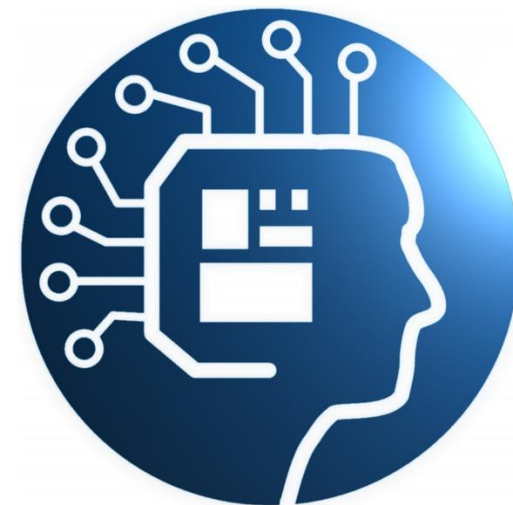


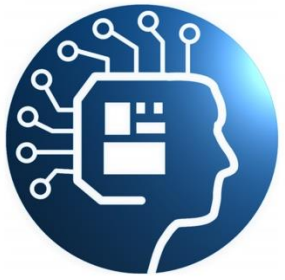
Zoom-in #4: Digital Placeability

- Results on 106 PnR runs from **47** designs, containing on average **42k** gates, targeting **BCD8sp** STMicro technology
- Methodology details: per-design data split, custom feature extraction and data augmentation, etc.



Lessons Learned



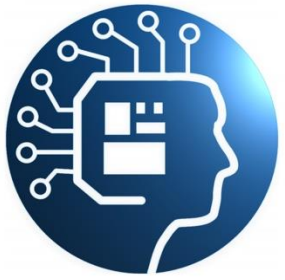


Lessons Learned

- After approximately 4 years, reflecting on the key challenges encountered when trying to implement an AI-centric project in the AMS IC design domain...
- Three key lessons learned:
 - 1. Transitioning from a research prototype to a practically usable tool is difficult**
 - 2. The “language barrier” can be hard to overcome.**
 - 3. IC companies still lack a real “data-driven” culture**

Disclaimers:

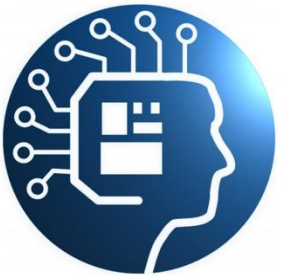
- Entirely personal view
- The industrial teams involved in AMBEATion did whatever they could to overcome these challenges



Lessons Learned

1. Transitioning from research prototype to “product”

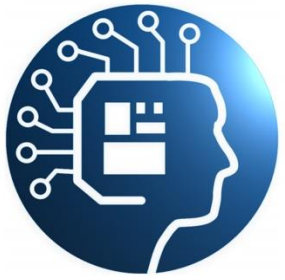
- Well-known problem for AI-based projects in other domains, particularly critical in this one
- Issues of **reliability/repeatability of results, computational cost, data quality/quantity** (see Lesson #3), **scalability, technology independence**, etc.
- But also, more practically:
 - Your design might achieve great metrics but still not “look good” to an analog designer (missing constraints, or just “artistic preference”)
 - Compatibility with industrial EDA flows is key for adoption, and not easy to achieve.



Lessons Learned

2. The “language barrier” can be hard to overcome.

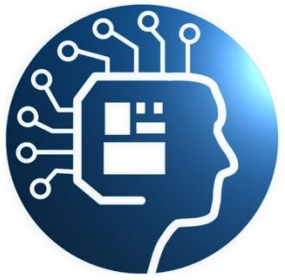
- Very few people have expertise in both AI/ML and IC design (especially analog)
- Experts in each of the two domains speak very different languages.
- Analog design choices can sometimes be difficult to formalize as algorithmic/quantitative. Maybe that’s why AI could work?
- **MSCA-RISE initiatives exist for this exact purpose!**



Lessons Learned

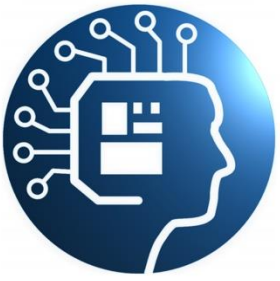
3. IC companies still lack a real “data-driven” culture

- AI/ML algorithms are extremely data hungry
- High-quality augmented/synthetic data generation is non-trivial
- Collecting data with sufficient **quantity** and **quality** has proven extremely difficult.
 - **Siloed projects/teams**, no centralized data infrastructure
 - Data deemed unuseful often overwritten.
- Example: Digital Placeability ML model trained on **85 passing, 21 failing** designs.
 - Data imbalance issue.



Conclusion

- Lots remain to be done to integrate ML techniques in EDA (especially for analog/AMS).
- AMBEATion's results, while preliminary, can hopefully motivate future research efforts in this area...
- ...and provide useful 'guidelines' for IC companies to develop their future AI-centered agenda (see later talks).



Questions?

Contact: daniele.jahier@polito.it

Selection of Project Publications:

- G. E. Aliffi et al., "AMBEATion: Analog Mixed-Signal Back-End Design Automation with Machine Learning and Artificial Intelligence Techniques," DATE 2024
- F. Daghero et al., "Machine Learning-based feasibility estimation of digital blocks in BCD technology," IEEE DTTIS 2024
- G. Faraone et al., "Machine Learning-based feasibility estimation of digital blocks for improved productivity in Analog-on-Top Back-End design flows", DAC 2024 (Industrial Session Poster).
- F. Daghero et al., ""Predicting Digital Layout Success in Analog-on-Top Designs using Machine Learning", IEEE NewCAS 2025 (in press).
- D. Barri et al., ""AMBEATion: New Algorithm for Generation IC Matched Structures with Respecting Linear and Non-linear Gradient Parameter Effects," IEEE AE 2024.