

Recent Trends in AI-assisted AMS IC Design

Free Online Workshop

July 21st, 2025, 15:00-17:00

Register [here](#). Access link will be sent after registration.

Program

15:00-15:20

Welcome Note - Lessons Learned from the AMBEATion Project

Daniele Jahier Pagliari, Politecnico Di Torino

15:20-15:40

Effective Analog ICs Floorplanning with Relational Graph Neural Networks and Reinforcement Learning

Davide Basso, University of Trieste

15:40-16:00

Learning to Act like a Pro: Discovering Procedural Models of Expert Workflows for Assistance and Validation

Antonino Furnari, University of Catania

16:00-16:20

The AI Revolution in ST Design Flow

Michelangelo Grosso, ST Microelectronics

16:20-16:40

A Modern Solution for Analog/Mixed-Signal Design

Marco Inglardi, Synopsys

16:40-17:00

A Follow-up to the AMBEATion Project

Dalibor Barri, ST Microelectronics

Workshop organised in the context of the
AMBEATion MSCA-RISE Project.

Contact: daniele.jahier@polito.it

The project has received funding from the European Union's Horizon 2020 research and innovation programme under the MarieSkłodowska-Curie grant agreement No 101007730. Results reflect only the author's view. The Agency is not responsible for any use that may be made of them.



15:00 - 15:20

Welcome Note

Lessons Learned from the AMBEATion Project

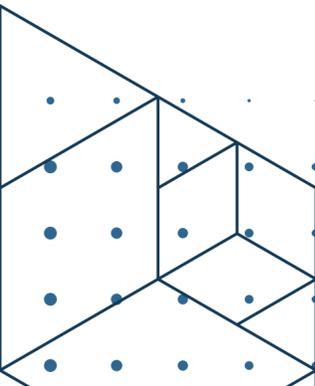
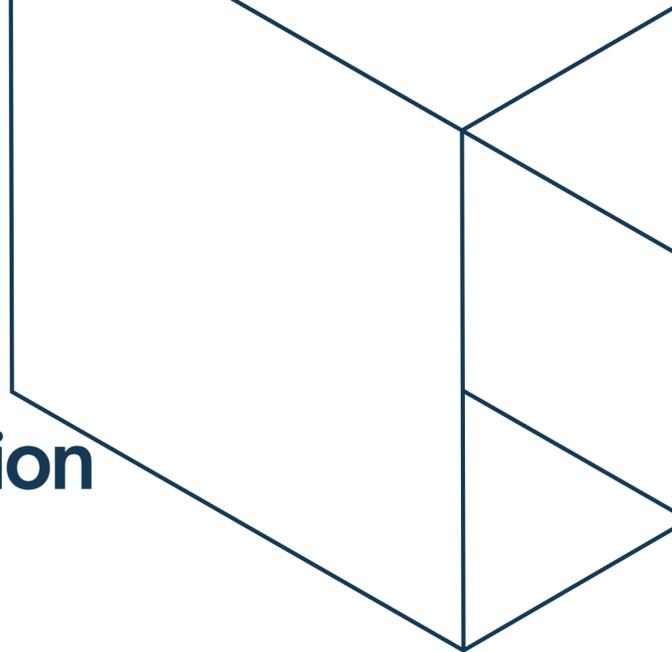
Daniele Jahier Pagliari

Politecnico di Torino

daniele.jahier@polito.it

Abstract: This talk will introduce and set the context for the online workshop, highlighting the motivations to pursue AMS design automation, the key open challenges, and the opportunities offered by AI technology in this domain.

We will then discuss lessons learned from the AMBEATion project (Analog/Mixed Signal Back End Design Automation based on Machine Learning and Artificial Intelligence Techniques), a Horizon 2020 MSCA-RISE initiative started in 2021, and aimed at creating links between Europe's research excellence in AI, EDA, and AMS design, and the know-how of key IC design industrial leaders such as Synopsys and STMicroelectronics. In particular, we will highlight the challenges encountered when transitioning from research "toy problems" to the complexity of a real industrial flow, and argue for the fundamental need of a more open "data-driven culture" in IC companies.



15:20 - 15:40

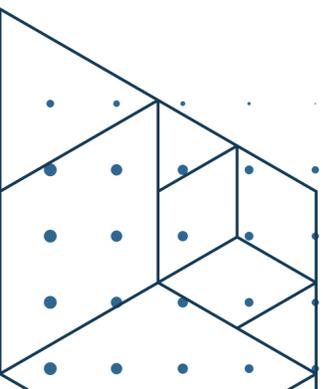
Effective Analog ICs Floorplanning with Relational Graph Neural Networks and Reinforcement Learning.

Davide Basso

University of Trieste

davide.basso@phd.units.it

Abstract: Analog IC floorplanning is a complex, manual process influenced by numerous constraints and high customization demands. In this presentation, we propose an automatic floorplanning algorithm using reinforcement learning combined with a relational graph convolutional neural network to encode circuit features and constraints. This method enables knowledge transfer across circuits with different topologies, improving generalization. Tested on 6 industrial circuits, it outperformed traditional techniques in speed, area, and wire length, achieving a 67.3% reduction in layout time and an 8.3% mean area reduction. This innovation streamlines layout creation through integration with procedural generators.



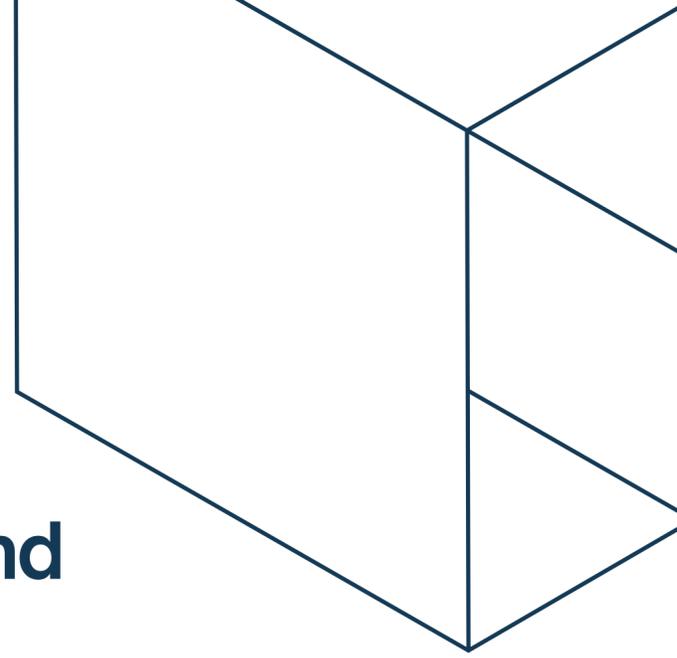
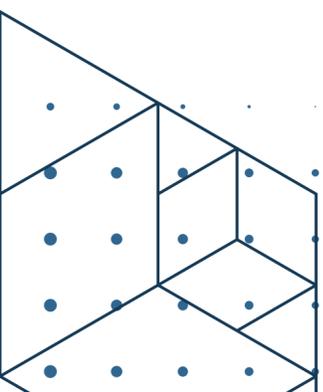
15:40 - 16:00

Learning to Act like a Pro: Discovering Procedural Models of Expert Workflows for Assistance and Validation

Antonino Furnari
University of Catania
antonino.furnari@unict.it

Abstract: The ability to perform complex, goal-oriented procedures is a hallmark of human expertise. In specialized domains, this expertise is a critical but often scarce resource, making the development of intelligent systems for assistance and workflow validation a primary goal. Traditional automation often relies on manually defined rules, which can be brittle and fail to capture the flexibility of expert behavior. To overcome this, we need methods that can learn procedural models directly from observing experts in action.

This talk explores three complementary paradigms for discovering such models from multimodal data. First, we present an approach to learn explicit, structured models by inducing task graphs from action sequences, providing an interpretable blueprint of the procedure. Second, we investigate the use of Large Language Models (LLMs) as implicit repositories of procedural knowledge, showing how they can be prompted to reason about task execution. Finally, we shift from modeling correctness to ensuring it, introducing an unsupervised paradigm that leverages gaze signals to identify procedural missteps, enabling real-time validation without predefined error taxonomies.



16:00 - 16:20

The AI Revolution in ST Design Flow

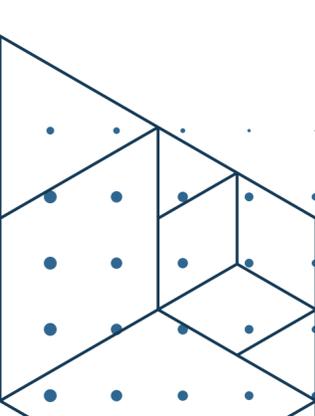
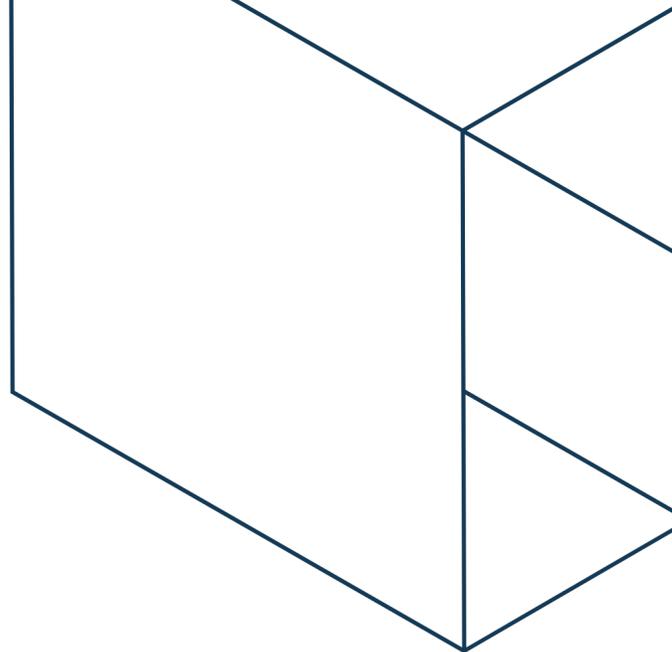
Michelangelo Grosso

ST Microelectronics

michelangelo.grosso@st.com

Abstract: At STMicroelectronics, we're fully embracing the AI revolution by integrating artificial intelligence throughout our entire design ecosystem. This includes everything from developing cutting-edge AI-capable hardware platforms to making it easy to deploy machine learning models on the STM32 microcontroller family. But we don't stop at hardware — we use AI to transform design processes across device, analog, and digital areas, helping to boost productivity and accelerate innovation at every step.

Our approach combines careful evaluation of the latest AI technologies from top EDA vendors and startups with the creation of customized AI-driven design methods tailored to ST's unique challenges. To bring all these efforts together and build a culture centered on AI, we have established the "AI in Design Flow" Affinity Working Group. This group encourages collaboration, sparks new ideas, and welcomes students, customers, and partners to join us in shaping the future of semiconductor design.



16:20 - 16:40

A Modern solution for Analog/Mixed Signal Design

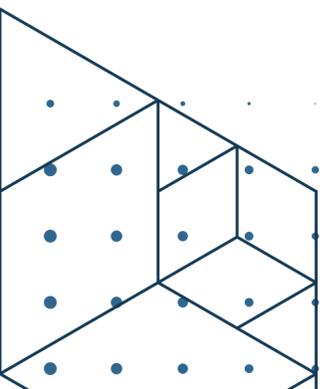
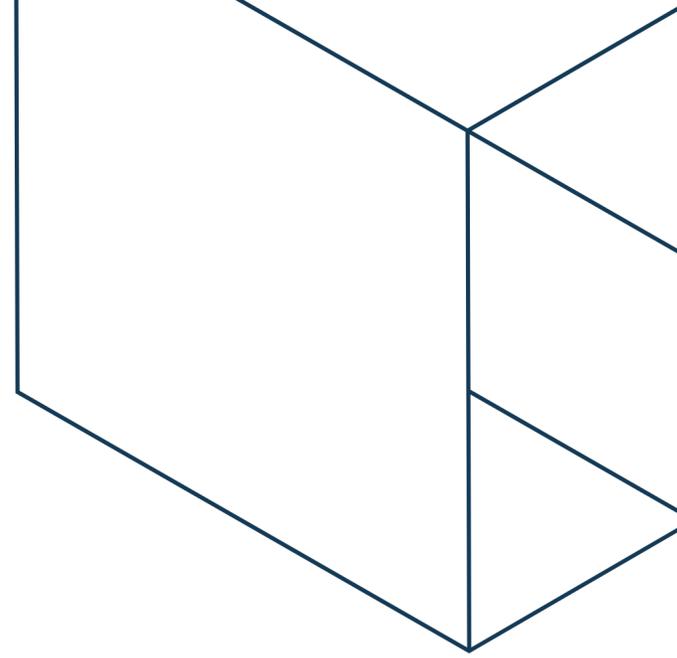
Marco Inglardi

Synopsys

marco.inglardi@synopsys.com

Abstract: This presentation will drive the audience through the complete AMS design and simulation platform. We will start with schematics creation and then move to PrimeWave, an open simulation environment, simulator agnostic and fully configurable through Python. We'll then talk about PrimeSim Continuum simulators family, spanning from foundry certified HSPICE engine for models validation to PrimeSim SPICE, the solution for SPICE parallelization, Cloud ready and GPU enabled, to FastSpice, including Mixed-Signal Verification.

We'll then move to Full Custom layout, introducing Custom Compiler, a full native OpenAccess layout solution with productivity boost through symbolic editing of layouts, pattern based router and template based layout. Custom Compiler is fully integrated with Physical Verification and Parasitics extraction, allowing in-design checks and partial layout extraction, as well as co-design with digital implementation. Design migration and optimization is also part of the platform through the new AI driven ASO.ai solution, allowing designer to fully migrate their projects between different silicon technologies.



16:40 - 17:00

A Follow-up to the AMBEATion Project

Dalibor Barri
ST Microelectronics
dalibor.barri@st.com

Abstract: This presentation will introduce a project that aims to revolutionize the design automation of analog-mixed-signal (AMS) integrated circuits by leveraging cutting-edge machine learning (ML) and artificial intelligence (AI) techniques. It represents a collaborative effort between leading academic institutions in Taiwan and Europe, including National Tsing Hua University, National Central University, Taiwan Tech, and Czech Technical University, and industry leaders such as STMicroelectronics and MicrolP.

The project focuses on developing innovative tools for automatic constraint generation, abstract layout generators, and a 2D AMS IC auto-placer that respects layout-dependent effects and supports hierarchical database structures. By integrating state-of-the-art methodologies and industry expertise, the project seeks to enhance the efficiency, accuracy, and commercial viability of AMS IC layout design.

